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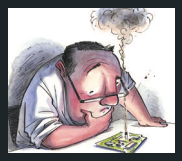

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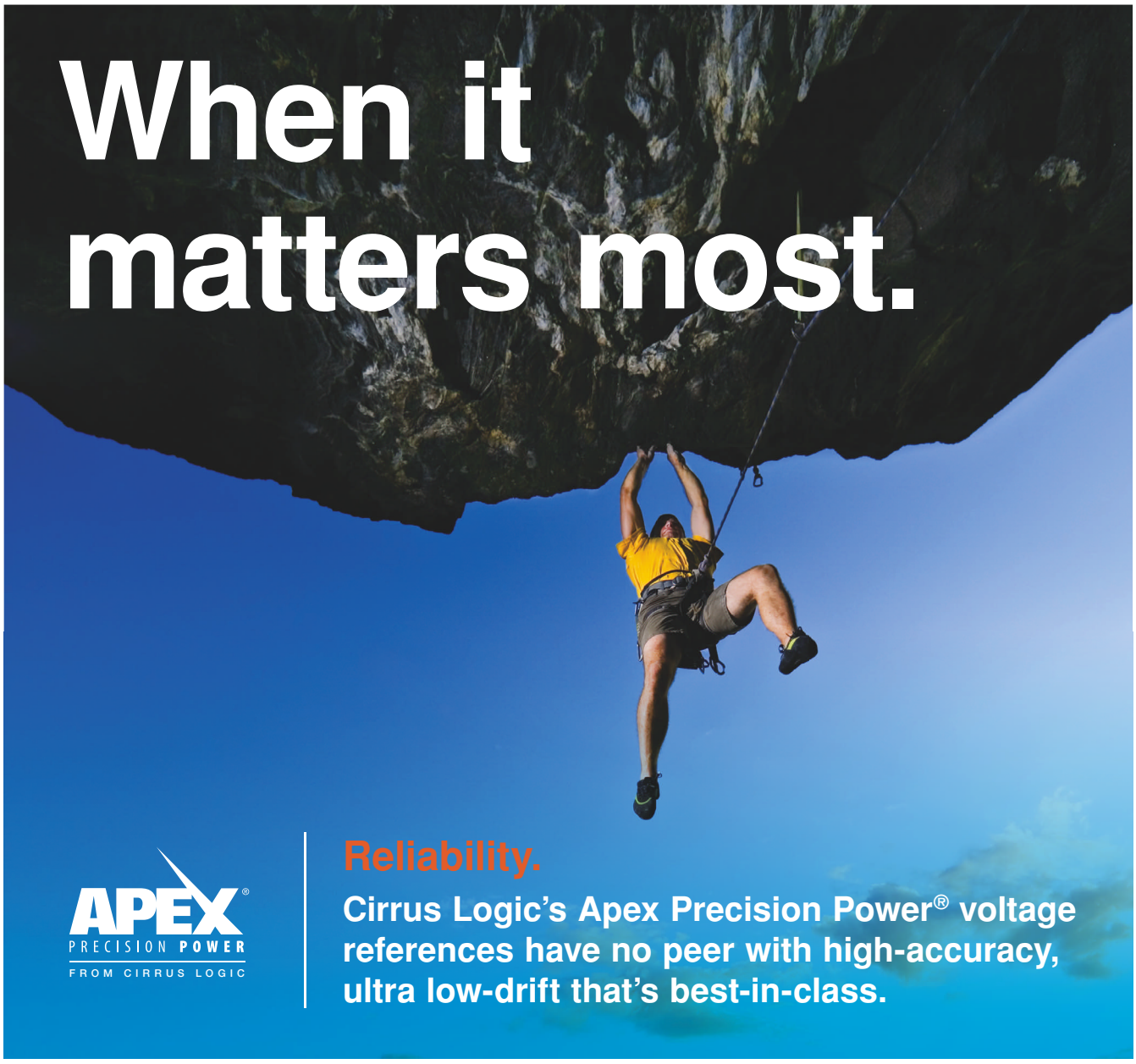

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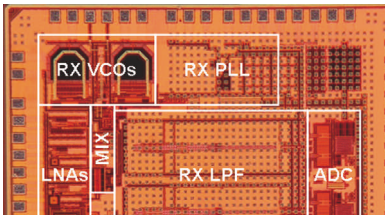
Sensors empower the "Internet of Things"

 Where are you? Who are you? What are you doing? Assume that someone or something—an individual, a company, or a government—knows the answer to all of these questions. Is this scenario a nightmare or the next obvious step to defining individuals in our society? Welcome to the "Internet of Things."

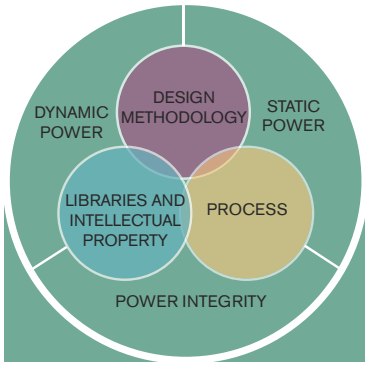
By Margery Conner, Technical Editor



Reconfigurable single-chip radios

 Extreme integration packs an extensive number of communications functions into a high-performance, low-area, low-power IC.

By Jan Craninckx and Piet Wambacq, IMEC



Power management for optimal power design

 A holistic approach to power management, from transistors to full-chip techniques, is necessary for meeting today's power-management goals.

By Prasad Subramaniam, eSilicon Corp

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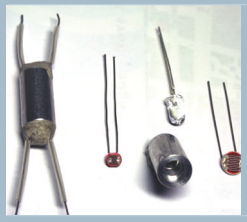

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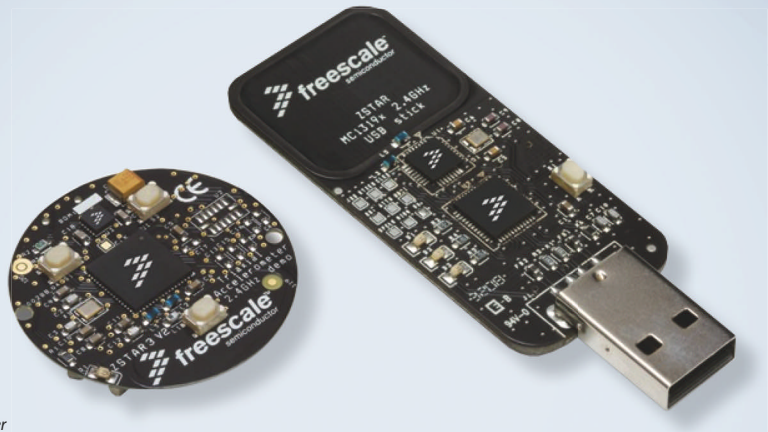

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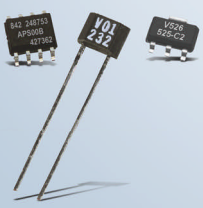

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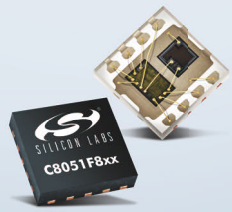

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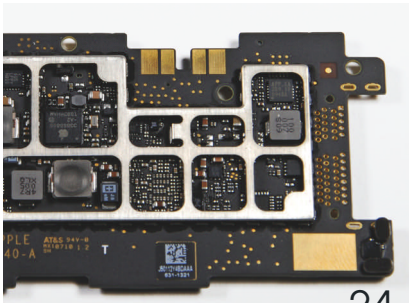

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Volume 55, Number 10 (printed in USA).

BY RON WILSON, EXECUTIVE EDITOR

MEMS, asynchronous logic enter SOC-design flow

Two companies that exhibited at the Embedded Systems Conference in San Jose, CA, in April have similar objectives but for different technologies. Coventor, a vendor of CAD and analysis tools for creating MEMS (microelectromechanical-system) devices, described a plan for bringing MEMS design into the standard CMOS SOC (system-on-chip) flow. Asynchronous-logic-design shop Tiempo showed a flow that facilitates development of large asynchronous blocks within a conventionally synchronous SOC.

Coventor provides MEMS-creation tools popular with specialists. C-Ware, for example, is a multiphysics simulator for modeling MEMS structures, and SEMulator is a 3-D-process-simulation tool for designing process steps to create the structures. Together with a 3-D-design-entry tool, the suite allows MEMS experts to create structures, investigate their behavior, and craft a manufacturing flow for them.

The next logical step, according to Michael Jamiolkowski, Coventor's president and chief executive officer, is to create behavioral models of the structures in C++ and electrical models in an accepted SOC-design environment and drop the designs into a library as reusable, parameterized IP (intellectual property). That task is the function of Coventor's new tool, MEMS+, a complete subflow for creating MEMS elements and integrating them into Cadence's Virtuoso.

MEMS+ includes a schematic generator and modeler, managers to handle materials and process data, a 3-D viewer, and layout and DRC (design-rule-checking) tools. Using this package, MEMS experts can create a new device design, along with a schematic symbol, an electrical netlist, a parameterized cell, DRC and LVS (layout-versus-schematic) data, and behavioral and electrical models for Spectre and UltraSim.

The emphasis in integration is slowly shifting toward integration of new kinds of devices that haven't previously been on the die at all.

In some ways, Tiempo's task is similar. The company's technology uses a data-encoding scheme to indicate to a receiving block when valid data arrives from the transmitting block. The approach requires an area overhead of 20 to 50% but significantly reduces both static and dynamic power; is virtually insensitive to pressure, voltage, and temperature variations; offers sharply reduced emissions; and can detect some security attacks.

Tiempo has for some time used the technology to produce IP, including a 16-bit microcontroller and a crypto-processor for contactless smart cards. Now, the company is offering a flow to make asynchronous design accessible to designers who don't know—and don't care to learn—the fine points of the technology. The flow begins with a transaction-level description of the desired block in SystemVerilog. Tiempo's tools synthesize the SystemVerilog code into a Verilog netlist, using a library of combinatorial and asynchronous cells. Verification is through either mixed-mode Verilog/SystemVerilog simulation or FPGA prototype.

The flow puts complex asynchronous blocks within the reach of ordinarily skilled SOC-design teams, according to Serge Maginot, Tiempo's president and chief executive officer. Designers need to learn only how to write a transaction-level model in which concurrent processes communicate through channels using read and write primitives, how to write interfaces between the asynchronous block and its synchronous surroundings, how to create timing constraints for the interface-resynchronization points, and how to create throughput constraints for the asynchronous paths.

In a way, both tool-flow announcements are signs of the times. The emphasis in integration is slowly shifting away from more gates, more memory, and more CPU cores and toward integration of new kinds of devices that haven't previously been on the die at all. The range and quality of passive components available to custom designers have been gradually increasing. Now, we are starting to see third-party tools for MEMS and for the asynchronous blocks that have long been the purview of only the largest and best-funded design teams in organizations such as Intel and IBM. More than Moore's Law is upon us. EDN

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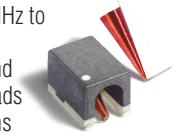

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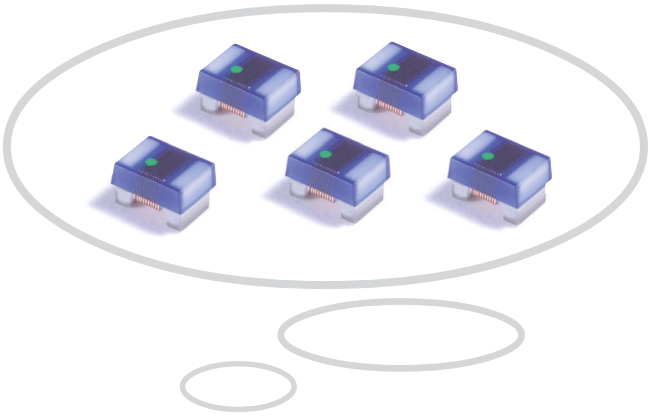

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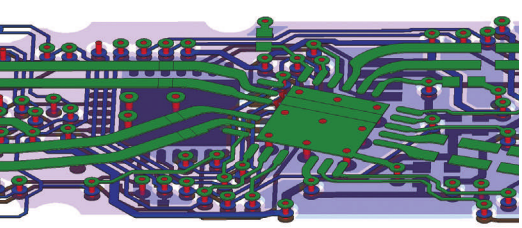

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INNOVATIONS & INNOVATORS

National Semiconductor, Silicon Labs team up for power-brick reference design

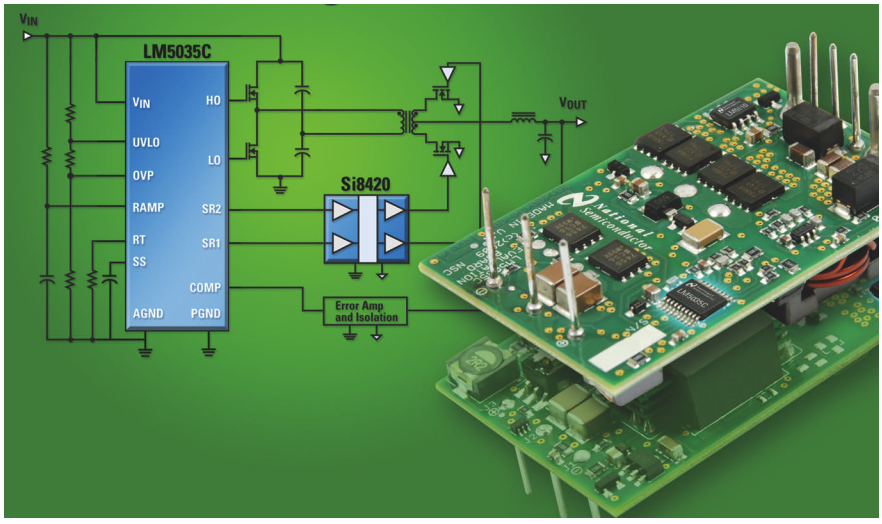
Silicon Laboratories and National Semiconductor have both contributed ICs to a power-brick reference design they co-developed. The brick uses a half-bridge architecture, with two FETs and two capacitors. The design targets use in networking, communications, and high-end server applications. It uses a National Semiconductor LM5035C PWM (pulse-width-modulation) controller and a Silicon Labs Si8420 isolator. The reference design produces 100W output power and comes in a 2.28×1.45×0.5-in. quarter-brick form factor. Input voltages to the brick can range from 36 to 75V, and it withstands 100V input transients. The board output is 3.3V at 30A, and efficiency is 89% at 30A and 92% at 15A output current.

Operating at a 400-kHz switching frequency, the device has a line regulation of 0.1% and load regulation of 0.2%. The six-layer design uses 2- and 3-oz copper on the outer and inner layers, respectively. It requires 200 cfm of airflow to maintain thermal integrity and offers both undervoltage lockout and overvoltage protection on the input bus. The PWM chip integrates 2A half-bridge gate drivers. The board's designers used the Silicon Labs isolator to send secondary-synchronous-rectification gate-drive signals across the isolation boundary. An LM8261 op amp drives an NEC (www.nec.com) PS2811 optocoupler to provide isolation for the feedback signal. The LM5035CEval board costs $135. The free reference-design files are available at National's Web site.

–by Paul Rako

▷**National Semiconductor**, www.national.com.

▷**Silicon Laboratories**, www.silabs.com.



National Semiconductor and Silicon Laboratories have teamed up to create a half-brick-power-supply reference design and evaluation board.

FEEDBACK LOOP

"Yes, we must continue to innovate, but it is important to not waste resources creating things that nobody wants."

—Engineer William Ketel, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6711874. Add your comments.

Energy-measurement chip meters power distribution units for server farms

"Smart power" usually brings to mind the smart power meters that will eventually sit at every business and home utility box and empower the smart grid. Another layer of applications for energy measurement exists, however: submetering, which measures power usage at the device or power-distribution level. A general utility meter measures power at the utility box when it comes into the facility—for example, a data farm. It next goes into a UPS (uninterruptible-power supply) and then on to the PDUs (power-distribution units), which act as smart power strips, sending the power to eight or as many as 64 channels, arriving ultimately at the power supplies in the servers themselves. At these huge megawatt installations, a variation of 1% in power efficiency is enough to win or lose business. However, without submetering at the PDU or power-supply level, the facility can't track power consumption to better than 5% accuracy.

The self-calibrating 78M6618 power-measuring SOC has an accuracy of greater than ±0.5% over a 2000-to-1 dynamic range.

To address these issues, the 78M6618 power-metering and -monitoring SOC (system on chip) from Teridian targets data-center PDUs as well as home and business smart power strips by enabling power metering, monitoring, and intelligent relay control of eight single-phase outlets simultaneously. You can control 32 or more channels by connecting multiple chips.

The 6618 has an accuracy of greater than ±0.5% over a 2000-to-1 dynamic range and includes self-calibration. It has a 22-bit delta-sigma ADC, 10 analog inputs, a precision voltage reference and digital temperature compensation. It includes a 32-bit computation engine, a microprocessor core, and flash memory. It sells for $5.90 (1000).

> If you're looking for real-time, accurate measurement, get an AFE, which costs about $1.

How does this pricing play in a world in which you can buy a Kill-a-Watt meter for $25? Jay Cormier, vice president of the energy-measurement division at Teridian, which Maxim-IC recently acquired, puts pricing in perspective: "If you're looking for real-time, accurate measurement, the only way to do it today is to get an AFE [analog front end], which costs about $1. For eight channels, you need eight AFEs, plus a microcontroller that adds another 50 cents. Plus, the AFEs require calibration. The 6618 comes with firmware, which takes out the development time. The chip is about half the cost of the component equivalent."

–by Margery Conner

▷**Teridian**, www.teridian.com.

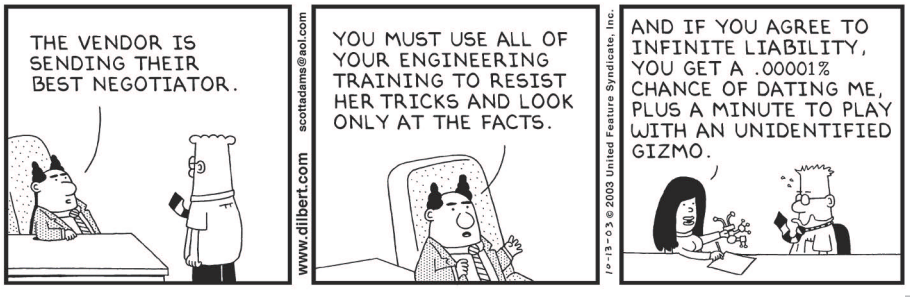
OLYMPUS AND CALIBRE SPEED CLOSURE

05.27.10

In recent process generations, routers have used design-rule data from LEF (library-exchange-format) files to check routes on the fly in an attempt to produce DRC (design-rule-checking)-clean routes. Unfortunately, there are approximately 1500 rules, prescribing nearly 6000 operations, at the 45-nm node, according to estimates from Mentor Graphics. Equally unfortunately, rules are emerging for which there are no provisions in LEF, so these rules are not available to the routing tools. The result is that routers are creating patterns that are not passing DRC–leading to iterations, frustrated rereading of the design rules, and manual routing of problem spots.

To address these issues, Mentor has introduced Calibre InRoute, an Olympus routing kernel that directly calls Calibre nmDRC, nmLVS (layout versus schematic), and DFM (design for manufacturing) to check its work. The mechanism is a dynamic API (application-programming interface) that allows Olympus, when it has satisfied the rules in the LEF file, to pass parameters to the Calibre routines and invoke them. Calibre then works directly on the Olympus data set. The tool requires no wholesale importing or exporting of data through ASCII files.–by Ron Wilson ▶Mentor Graphics, www.mentor.com.

DILBERT By Scott Adams



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Apple buys second chip company

Apple recently acquired Intrinsity, a leader in low-power, static design, for a rumored total of $121 million. Such an acquisition makes sense for the consumer-electronics leader because many in the industry suspect that Intrinsity is the CPU-core-technology provider for Apple's custom A4 microprocessor in the iPad. According to Linley Gwennap, founder and principal analyst of The Linley Group (www.linleygroup.com), Intrinsity engineers designed the company's Cortex-based Hummingbird processor under contract to Samsung (www.samsung.com), which manufactures the 1-GHz A4. "No one has announced a 1-GHz Cortex A8 CPU other than Samsung with the Hummingbird," he says.

The Intrinsity purchase follows Apple's 2008 purchase of PA Semi, a fabless chip designer that specialized in low-power PowerPC microprocessors, for $278 million. Some people initially thought that Apple relied on the acquired PA Semi team to build the iPad's A4 processor. Gwennap notes, however, that the scenario is unlikely because a CPU usually takes three years to design, integrate, and validate. As such, he believes, PA Semi's technology has not been part of Apple long enough to be a design factor in the iPad, which Apple officially announced in January 2010, less than two years after it acquired PA Semi. Gwennap in a February blog post instead suggested the Hummingbird was behind the iPad's A4. Since then, several industry analysts have pointed to Intrinsity as the key to the A4.

> "Apple likely had future A4 design plans beyond the iPad in mind when making the purchase.

Still, Apple may have had its PA Semi acquisition in mind when purchasing Intrinsity. "Intrinsity's real expertise is more in the circuit design," says Gwennap. The company has spent years developing and patenting techniques to achieve high clock speeds at low power, whereas PA Semi's expertise is in more of the CPU-architecture and -logic design. "[Apple] could use the Intrinsity circuit techniques to accelerate whatever CPU architecture the PA Semi guys have been working on," he says. "They could fit together pretty well."

Apple also likely had future A4 design plans beyond the iPad in mind when making the purchase. "It doesn't really make sense for Apple to invest this much money to develop CPUs for the iPad," Gwennap says. "The product sales are supposed to be in the millions this year, but they have a large and thriving iPhone business, so I would fully expect the A4 to be in the next-generation iPhone and potentially in the iPod touch, as well. When you put the three products—the iPad, iPhone, and iPod touch—together, you're looking at a 50 million run rate. That's the kind of run rate that makes sense to design a custom processor for."**–by Suzanne Deffree**

▷**Apple Computers Inc**, www.apple.com.

REDPINE, RENESAS TEAM ON EMBEDDED WI-FI

The notion of using Wi-Fi as a data-communications link in embedded systems has both appeal and complexity. Obviously, 802.11 is ubiquitous, mature, and well-understood, and inexpensive silicon abounds. Wi-Fi's developers, however, never intended it for mission-critical links. It is nondeterministic and not energy-efficient, and it requires trained operators to set up and maintain connections. It also requires certification from both the Federal Communications Commission (www.fcc.gov) and the Wi-Fi Alliance (www.wi-fi.org).

To address these issues, Redpine Signals has teamed with Renesas Electronics, combining Redpine's 802.11n module with your choice of several Super-H, RX, and R8C Renesas microcontrollers to offer plug-and-play embedded Wi-Fi. According to Venkat Mattela, chief executive officer of Redpine, the move to 802.11n resolves many of the issues with embedded Wi-Fi, and he believes that single-stream 11n is inherently robust and energy-efficient, significantly improving Wi-Fi's suitability for embedded use. "For embedded designers, the experience out of the box is vital," he says. "You can't assume the design will have a 2-GHz CPU or that your customer is willing to port a protocol stack to it. You can't assume a PC-knowledgeable person will be there to install the end system. Embedded Wi-Fi has to work with the designer's application, right out of the box."

To this end, Redpine's SOC (system on chip)–the base of the module–includes a proprietary CPU core targeting low-power execution of 802.11n protocol stacks. The baseband code, MAC (media-access control), TCP/IP (Transmission Control Protocol/Internet Protocol), and Wi-Fi Supplicant all reside on the SOC. The only required external software is a 2-kbyte driver on the external microcontroller. The module combines the SOC, power and RF components, and an antenna, so it is an out-of-the-box hardware/software package, carrying FCC and Wi-Fi certifications.

To minimize energy consumption, Redpine has both exploited the energy-conserving features of .11n and employed current thinking on low-power design. For example, the SOC uses the interval between packets to reduce the sample rate on the signal-chain ADC and uses the fact that the protocol stack runs locally on the chip to deduce opportunities to shut down blocks.

All this work gives the SOC a low energy profile. Redpine claims that the chip reaches 10 µW in deep sleep and can remain operating at a supply of less than 3 mW. An active 115-kbps link, such as you would use to carry SPI (serial-peripheral-interface) traffic, requires less than 30 mW.

–by Ron Wilson

▶Redpine Signals, www.redpinesignals.com.

▶Renesas Electronics, www.renesas.com.

05.27.10

3-D system uses optical fiber to provide new options for photovoltaics

Researchers at the Georgia Institute of Technology have grown zinc-oxide nanostructures on optical fibers and coated them with dye-sensitized solar-cell materials to develop a new type of 3-D PV (photovoltaic) system. The approach could allow scientists to hide PV systems from view and locate them away from traditional locations, such as rooftops. "Using this technology, we can make photovoltaic generators that are foldable, concealed, and mobile," says Zhong Lin Wang, a Regents professor at the Georgia Tech School of Materials Science and Engineering. "Optical fiber could conduct sunlight into a building's walls, where the nanostructures would convert it to electricity. This is truly a 3-D solar cell."

An article in *Angewandte Chemie International* details the researchers' findings (**Reference 1**), which DARPA (Defense Advanced Research Projects Agency, www.darpa.gov), the KAUST (King Abdullah University of Science & Technology Global Research Partnership (www.kaust.edu.sa/research/grc.html), and the National Science Foundation (www.nsf.gov) sponsored.

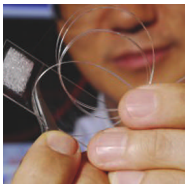
The researchers employed dye-sensitized solar cells, which use a photochemical system to generate electricity. They are inexpensive to manufacture, flexible, and mechanically robust, but their trade-off for lower cost is conversion efficiency lower than that of silicon-based cells. Using nanostructure arrays to increase the surface area available to convert light could help reduce the efficiency disadvantage, however, and give architects and designers new options for incorporating PV into buildings, vehicles, and even military equipment.

Fabrication of the new Georgia Tech PV system begins with the same type of optical fiber the telecom industry uses to transport data. First, the researchers remove the cladding layer. They then apply a conductive coating to the surface of the fiber before seeding the surface with zinc oxide. Next, they grow aligned zinc-oxide nanowires, much like the bristles of a bottle brush, around the fiber. They then coat the nanowires with the dye-sensitized materials that convert light to electricity.

Sunlight entering the optical fiber passes into the nanowires, where it interacts with the dye molecules to produce electrical current. A liquid electrolyte between the nanowires collects the electrical charges. The result is a hybrid nanowire/optical fiber system that can be as much as six times as efficient as planar zinc-oxide cells with the same surface area. "You have multiple light reflections within the fiber and multiple reflections within the nanostructures," Wang says. "These interactions increase the likelihood that the light will interact with the dye molecules, and that [process] increases the efficiency."

Researchers grow a brown, light-absorbing material for the solar generators on optical fiber (courtesy Gary Meek, Georgia Tech).

Researchers Benjamin Weintraub (left), Zhong Lin Wang (center), and Yaguang Wei (right) examine an image of their 3-D solar cell (courtesy Gary Meek, Georgia Tech).



Georgia Tech Regents professor Zhong Lin Wang holds a prototype 3-E solar cell that could allow designers to locate PV systems away from rooftops (courtesy Gary Meek, Georgia Tech).

Wang and his team have reached an efficiency of 3.3% and hope to reach 7 to 8% after surface modification. Although lower than the efficiency of silicon solar cells, this efficiency would be useful for practical energy harvesting. If the researchers can achieve that goal, the potentially lower cost of their approach could make it attractive for many applications.

By providing a larger area for gathering light, the technique would maximize the amount of energy that strong sunlight produces and generate respectable power levels even in weak light. Using lenses to focus the incoming light could increase the amount of light entering the optical fiber, and the fiber-based solar cell has high saturation intensity. This new structure will offer architects and product designers an alternative PV format for incorporating into other applications. "We could eliminate the aesthetic issues of PV arrays on buildings," says Wang. "We can also envision PV systems for providing energy to parked vehicles and for charging mobile military equipment where traditional arrays aren't practical."

Wang and his team have produced generators on optical fiber as long as 20 cm. "The longer the better because the longer the light can travel along the fiber, the more bounces it will make and the more it will be absorbed," says Wang. The researchers have been using traditional quartz optical fiber, but Wang would like to use less expensive polymer fiber to reduce the cost.

Although the cells could find use in large PV systems, Wang doesn't expect them to soon replace silicon devices. He does, however, believe that they will broaden the potential applications for photovoltaic energy. "This [approach] is a different way to gather power from the sun," Wang says. "To meet our energy needs, we need all the approaches we can get."

–by Fran Granville

▷**Georgia Institute of Technology**, www.gatech.edu.

REFERENCE

1 Weintraub, Benjamin, Yaguang Wei, and Zhong Lin Wang, PhD, Optical Fiber/Nanowire Hybrid Structures for Efficient Three-Dimensional Dye-Sensitized Solar Cells," *Angewandte Chemie International,* Volume 48, Issue 7, Oct 22, 2009, pg 8981, www3.interscience.wiley.com/journal/122659616/abstract.

VOICES

The MathWorks' Silvina Grad-Freilich talks high-performance computing

The HPC [high-performance-computing] market will resume growth in the middle of this year, although change will be evolutionary, according to "IDC's Top 10 HPC Market Predictions for 2010," which the company presented earlier this year. To learn how HPC might affect the design community, *EDN* spoke with Silvina Grad-Freilich, parallel-computing marketing manager at The MathWorks.

What does The MathWorks offer that can help designers take advantage of HPC?

A We have a set of tools called the Parallel Computing Toolbox, and these tools allow you to solve larger problems by using additional compute capacity. That additional compute capacity can be anything from the multiple cores in your desktop machine to clusters or grids. A second toolset is Matlab Distributed Computing Server, which allows users to scale the applications they develop to run on a cluster.

How can Matlab and Simulink users employ these tools?

A Matlab users usually write their own code, but one of the premises is that they are domain experts more than programmers. One of the main reasons they came to Matlab is to basically have a development environment where they can rapidly develop a prototype. One of the things that these parallel-computing tools allows them to do is stay in the same environment.

What other support do you offer for parallel computing?

A We have integrated other toolboxes with the Parallel Computing Toolbox. In the Statistics Toolbox and Optimization Toolbox, for example, there are already some functions we have parallelized. So if you write an application based on those functions, you don't need to change your application at all to be able to use all the cores in your machine or scale your application up to a cluster.

In addition to that feature, we provide APIs [application-programming interfaces] so that you as a Matlab user can also parallelize your own applications. For example, let's suppose that you have an application such as a parameter sweep or a Monte Carlo simulation that tests Matlab code over a set of parameters. In Matlab, that would be expressed by a for loop. To parallelize the application, you just change the for loop to a parfor loop.

And what about Simulink?

A Something very similar happens to Simulink. For example, the Simulink Design Optimization tool also works with the Parallel Computing Toolbox. With parallel computing integrated within Design Optimization, you can make use of the different cores in your machine or a cluster to run more simulations.

IDC predicts that x86 processors will dominate but GPUs (graphics-processing units) will gain traction. Does The MathWorks support GPUs?

A Not yet, but we have a beta program running right now that started at the beginning of this year. Basically, we are inviting Matlab users to test our solution for GPUs. The program has been amazingly popular within our customer base.

Were there any surprising predictions raised in the IDC presentation?

A Not surprising, but interesting. One prediction is about how the challenge of highly parallel programming will increase, and we as programmers have seen all the time that programming a multicore machine is significantly harder than programming for a single-core machine, but what we are trying to do with our tools is to shield users from that complexity.

What else did you take note of in the predictions?

A One of the predictions is that the HPC market will resume growth in mid-2010. That prediction is great to see. One thing we have said is that, during the recession and even now, our tools have been very successful. Even with all the changes in the economy and the recession and layoffs, people are looking for more and more ways to be more productive, and running our tools on high-performance computers is all about productivity.

–interview conducted and edited by Rick Nelson

RAQ's

Rarely Asked Questions

Strange stories from the call logs of Analog Devices

Keeping Your A/D Converter Clocks Jitter Free

Q. How do I make improvements to my system clock or clock circuit so as to reduce jitter?

A. Jitter or noise on a clock signal can only corrupt an ADC's timing when present around the threshold region of the ADC's clock input. Increasing the slew rate of the clock signal decreases its transition time, thus reducing the amount of time that noise is present during the threshold period. This effectively reduces the amount of rms (root-mean-square) jitter introduced to the system. As an example, a 12-bit ADC requiring 100-fs minimum rms jitter for a 70-MHz analog input must have 1-V/ns slew rate.

So, minimizing jitter means improving the slew rate of the clock edge. One way to do this is to improve the clock source itself. A custom high-performance clock oscillator is typically used to characterize the baseline performance achieved by Analog Devices ADCs. Not all users of these high-speed converters can afford the cost or space required by a high-performance, oven-controlled, low-jitter oscillator, but available cost effective oscillators can achieve reasonable performance, even at high input frequencies. Care should be taken when selecting an "off-the-shelf" oscillator, though, as oscillator vendors do not always specify or measure jitter in the same way. A pragmatic way to determine which oscillator is best for the particular application is to collect a handful and test them in the system directly. By making this choice the only variable, performance can be predicted (assuming that the oscillator vendor maintains reasonable standards of quality control). Better yet is to contact the oscillator manufacturer to obtain

jitter- or phase noise data and get suggestions as to how to best terminate the device. Improper oscillator termination can seriously degrade the converter's spurious-free dynamic range (SFDR).

It is critical to understand the entire clock system in order to achieve the best possible performance from the converter. Decreasing the jitter of the system clock circuit can be achieved in many ways, including improving the clock source, as discussed, as well as filtering, frequency division, and proper choice of clock circuit hardware. Remember to pay attention to the slew rate of the clock, as this will determine the amount of noise that can corrupt the converter during the transition time. Minimizing this transition time can improve the converter's performance. Use only necessary circuitry to drive and distribute the clock because each component in the signal chain will increase the overall jitter. Finally, don't use "cheap" hardware; its performance is likely to be disappointing. One can't expect championship performance from a $70,000 car outfitted with $20 tires.

To Learn More About Jitter Free Clocks
http://designnews.hotims.com/27744-101

Contributing Writer Rob Reeder is a senior converter applications engineer working in Analog Devices high-speed converter group in Greensboro, NC since 1998. Rob received his MSEE and BSEE from Northern Illinois University in DeKalb, IL in 1998 and 1996 respectively. In his spare time he enjoys mixing music, art, and playing basketball with his two boys.

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BY BONNIE BAKER

The best solution brings accuracy

In my last article, I compared the throughput times of SAR (successive-approximation-register) and delta-sigma ADCs (**Reference 1**). I concluded that the throughput times—70k and 24k samples/sec—of PGA (programmable-gain-amplifier)-SAR systems and delta-sigma converters, respectively—are close. Which system is best? It looks like a draw with this evaluation, but what about accuracy?

Think of accuracy in terms of whether a system can produce the right output value. You can best describe the system accuracy with the dc specifications, such as offset, gain, and linearity. In this evaluation, use the appropriate system devices' minimum or maximum specification.

Once you refer the offset errors of each device to the input of each device, you can add them together. The equation for this calculation is available with the online version of this article at www.edn.com/100527bb. In a similar fashion, you can calculate a system's RTI (referred-to-input) gain error and linearity error.

Usually, you combine the uncorrelated dc errors, of gain, offset, and linearity, using an RSS (root-sum-square) formula. The equation for this calculation is available with the online version of this article at www.edn.com/100527bb. Note that you should refer these errors to the system input.

In general, an SAR ADC's accuracy, or TUE (total unadjustable error), becomes worse with increased gain. This statement may not intuitively make sense, but remember that two factors are at work. First, increasing PGA gain decreases the system input's full-scale voltage range, and actual voltage LSB for 12-bit systems. Second, the absolute voltage errors from the op amp and ADC decrease. Unfortunately, the PGA offset voltage error remains constant.

Now consider a delta-sigma converter's TUE characteristics. Many readers of a previous column suggest that the delta-sigma units win out over PGA-SAR systems (**Reference 2**). As with any other ADC, delta-sigma converters generate the offset, gain, and linearity dc errors. The key difference between applying a process gain with a delta-sigma converter and applying an analog gain with a PGA-SAR circuit is that the process gain does not multiply the offset error. On the other hand, the gain and linearity error is inversely proportional with increases in process gain. The end result is that the TUE decreases with increases in process gain. However, the TUE as a percentage of full-scale range remains constant.

For discussion purposes, **Table 1** compares data from a PGA-SAR system and from a delta-sigma converter. The PGA-SAR system comprises the PGA116 PGA, the OPA350 operational amplifier, and the 12-bit ADS7886 ADC. The delta-sigma converter is the 24-bit ADS1258. In this evaluation, neither system performs to a 12-bit accuracy level, but the PGA-SAR combination is generally more accurate than the delta-sigma converter.

I challenge you to find two systems with comparable throughput rates in which the PGA-SAR system is generally less accurate than the delta-sigma converter over their entire gain ranges. Send your ideas to me at ti_bonnie baker@list.ti.com. EDN

For the references cited in this column, go to www.edn.com/100527bb.

TABLE 1 COMPARISON OF CONVERTER PERFORMANCE

Baseline			PGA SAR		Delta Sigma	
Analog or process gain	System full-scale range (V, RTI)	System LSB size (μV, RTI)	TUE (μV, RTI)	TUE percentage of full-scale range	TUE (μV RTI)	TUE percentage of full-scale range
One	5	1220.7	8701	0.174	25,000	0.5
Two	2.5	610.35	4368	0.175	12,500	0.5
Four	1.25	305.18	2203	0.176	6250.01	0.5
Eight	0.625	152.59	1121	0.179	3125	0.5
16	0.3125	76.29	583	0.187	1552,54	0.5
32	0.1563	38.15	319	0.204	781.33	0.5
64	0.0781	19.07	194	0.248	390.78	0.5
128	0.0391	9.54	138	195.63	195.63	0.501

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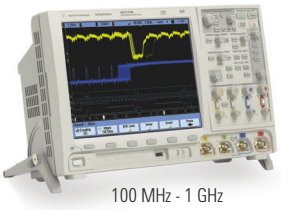
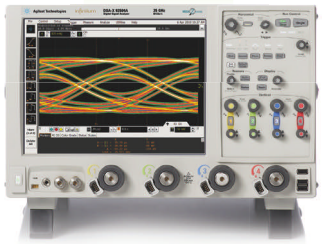


100 MHz - 1 GHz

2.5 GHz - 13 GHz



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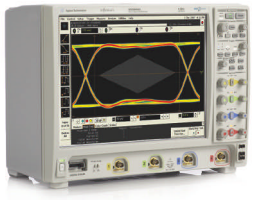

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BY PALLAB CHATTERJEE, CONTRIBUTING TECHNICAL EDITOR

Nanopatterning: getting the right objects small

The new materials and new phenomena that result from size are driving nanotechnology applications. One of the major challenges is creating these tiny objects in the shape and orientation to have control over these new characteristics. The leading methods of patterning at the nanoscale dimensions of 1 to 100 nm are lithography, nanoimprinting, and self-assembly.

Designers have traditionally preferred lithography for IC and MEMS (microelectromechanical-system) design and creation. Optical lithography uses a series of lenses and a single light source to project a tiny image of a scaled master image on a mask onto the substrate, which, in most cases, is a silicon wafer.

Discussions abound about when EUV (extreme-ultraviolet) lithography with a short-wavelength light source will replace optical lithography. Nevertheless, the use of double patterning, immersion lithography, and other multiple-imaging techniques is pushing 193-nm lithography to 32- and 28-nm processes. Manufacturers such as Nikon have recently introduced lithographic equipment for the double-patterning applications. These techniques dominate the semiconductor arena due to their high throughput and systematic predictability of the output images.

Image patterning down to 25 nm is now possible at high throughput using nanoimprinting technology (**Figure 1**). These features can be complicated for both IC and hard-disk-drive applications. For production, manufacturers must print these features on both sides of the hard-drive platter. Nanoimprint technology provides a physical contact and may include J-FIL (jet-and flash-imprint-lithography) technology, which uses a UV-flash exposure with an intelligent, pattern-density-based resist-drop-pattern deposition system. The high throughput requires high-quality master plates, with high accuracy and long manufacturing times using a Gaussian e-beam writer, and low-cost, high-resolution "working plates."

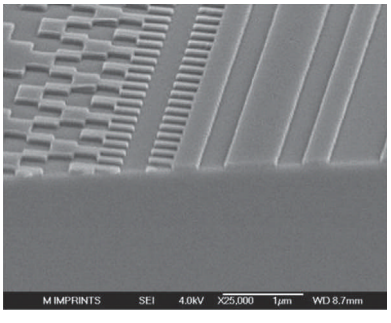

Figure 1 Image patterning down to 25 nm is now possible at high throughput using nanoimprinting technology.

Manufacturers such as Molecular Imprints have recently introduced machines for the high-speed, low-cost creation of these working plates, extending the nanoimprint technology to traditional CMOS-silicon-wafer fabrication and to ultra-high-volume nanomedical applications. The working plates become the tools for the nanoimprinting machines that create patterns on the wafers.

The third leading method is block-copolymer self-assembly, in which a machine simultaneously introduces multiple polymer chains of different materials to a surface. The polymers' interaction creates systematic, 3- to 50-nm patterns without any pattern postprocessing. The patterns are typically cylinders, circles, lines, or rings, depending on the density of materials. Researchers intend to use these patterns for electronics, in contacts and interconnect for the 16-nm and smaller nodes, as well as for solar and nanomolecular applications. The solar applications are seeking higher-efficiency absorption patterns, which in turn will result in high-efficiency solar cells.

IC fabrication has been relying on lithographic processes since its inception in the early 1950s, and the technology is well-developed down through 45-nm geometries. Work is under way to push lithography from 45 to 16 nm. Nanoimprint technology has also been around for a while. It is in its third or fourth generation of equipment and materials and is starting to take prominence in the hard-disk-drive markets as they approach terabit-per-square-inch densities. Current patterning is pushing this level with research to increase this figure to 10 Tbps/in.^{2}. Self-assembly is still in the research stage and best suits systems using 16-nm and smaller lithographies, including the nanomedical market. EDN

Pallab Chatterjee is vice chairman of the IEEE San Francisco Bay Area Nanotechnology Council. You can reach him at pallabc@siliconmap.net.

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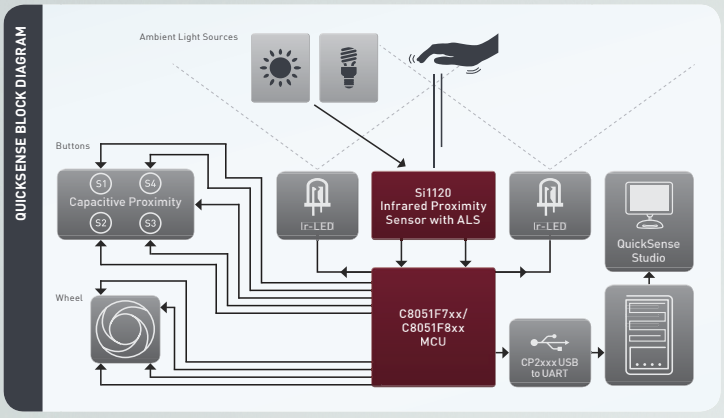

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Apple's iPad: new computing form factor or passing fad?

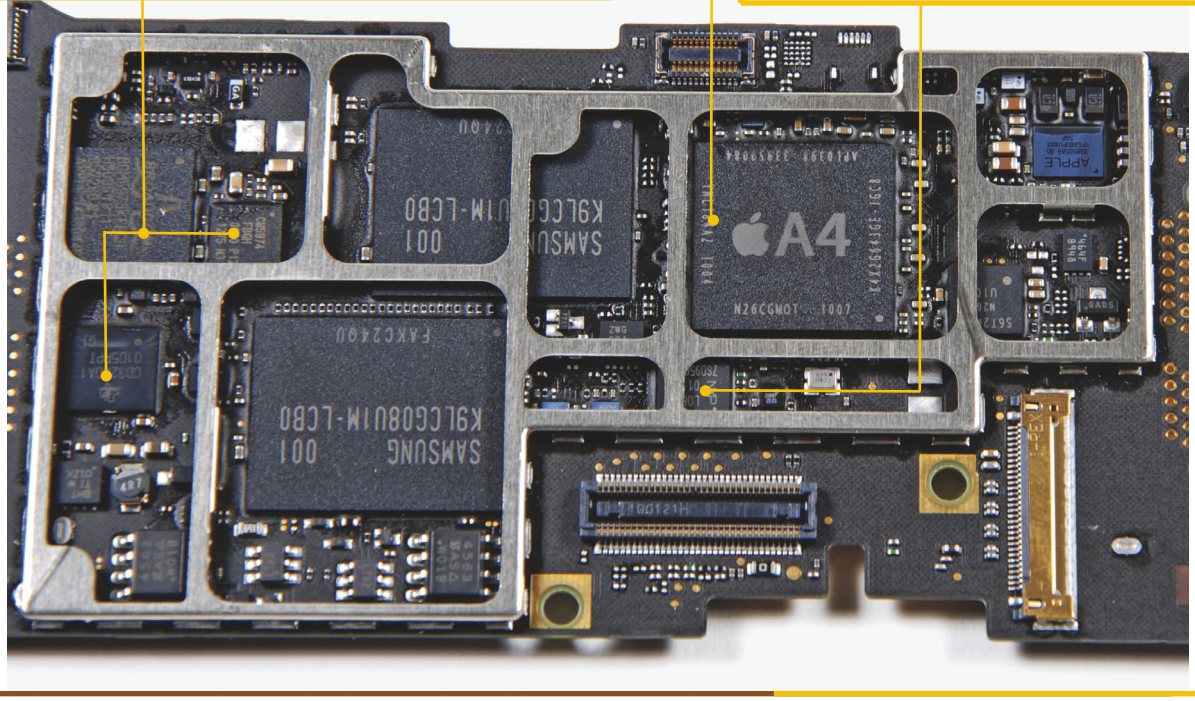
Tablet-style computers running both Unix and Windows operating systems have for many years been an enduring presence on the tech landscape, primarily by virtue of the innumerable product failures. In early April, Apple began selling its first-generation OS X-based iPad. Is Apple's tablet destined for greater success than its predecessors, and what hardware building blocks compose it? My friends at iFixit (www.ifixit.com/Teardown/iPad-Teardown/2183/1) helped me answer these questions.

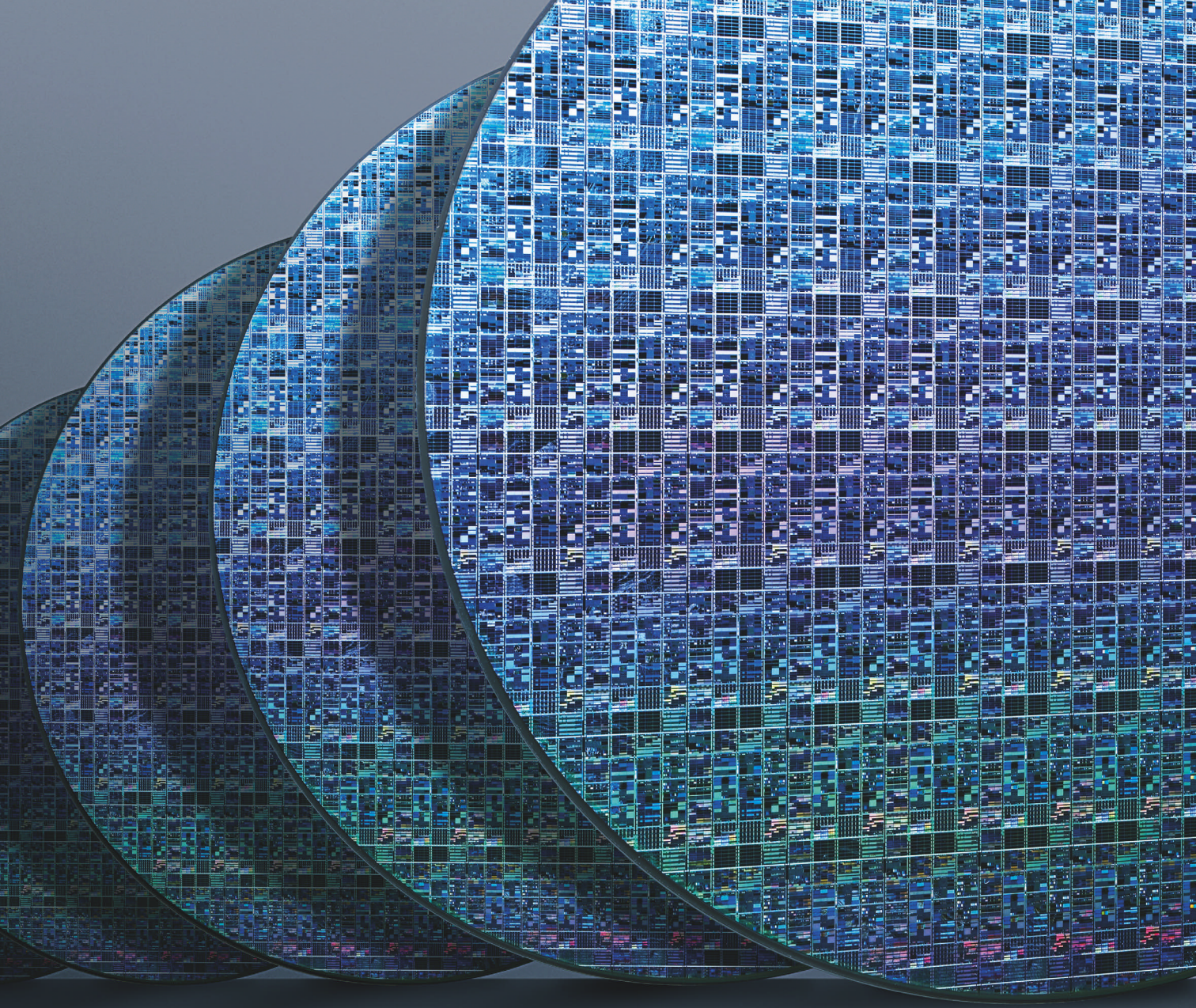
At approximately 4.5 in. wide, the iPad's primary PCB (printed-circuit board) is about the same size as that in an Apple handheld device, leaving plenty of room in the system cavity for the 25-Whr lithium-polymer battery. With the iPad, Apple also used many of the same chips it used in both the iPod touch and the iPhone, thereby giving a measure of validity to the oft-repeated observation that the iPad is little more than a big iPod touch.

Die analysis and software profiling both suggest that the 1-GHz, ARM-based Apple A4 microprocessor combines a Cortex A8 single-core CPU and a PowerVR SGX 535 graphics processor. Although Apple more than two years ago bought PA Semiconductor—notably, the company's ARM-design expertise—persistent rumor suggests that Intrinsity, which Apple reportedly also acquired, spearheaded this project. The package also includes two 1-Gbit Samsung DRAM die, for 256 Mbytes of total system memory, the same amount as the latest-generation iPod touch.

The display interface employs Broadcom's BCM5973 microcontroller IC and BCM5974 capacitive-touchscreen-controller IC, plus Texas Instruments' CD3240A touchscreen-line-driver IC, rather than a more leading-edge approach with greater integration. This design choice likely reflects the fact that the iPad has a larger, higher-resolution screen than does either the iPhone or the iPod touch. It also has comparatively more PCB real estate.

Other notable ICs include an NXT-developed DisplayPort and PCIe (Peripheral Component Interconnect Express) multiplexer/demultiplexer and an STMicroelectronics-supplied accelerometer. The identity and location of the silicon compass, an IC that made its debut in Apple's product line with the iPhone 3GS, are currently unknown. More generally, Apple's insistence on employing proprietary package markings complicates function and sourcing identification of many devices inside the iPad.





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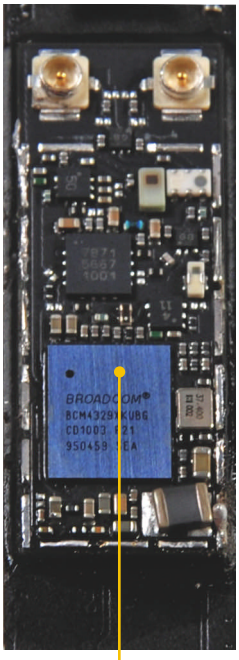
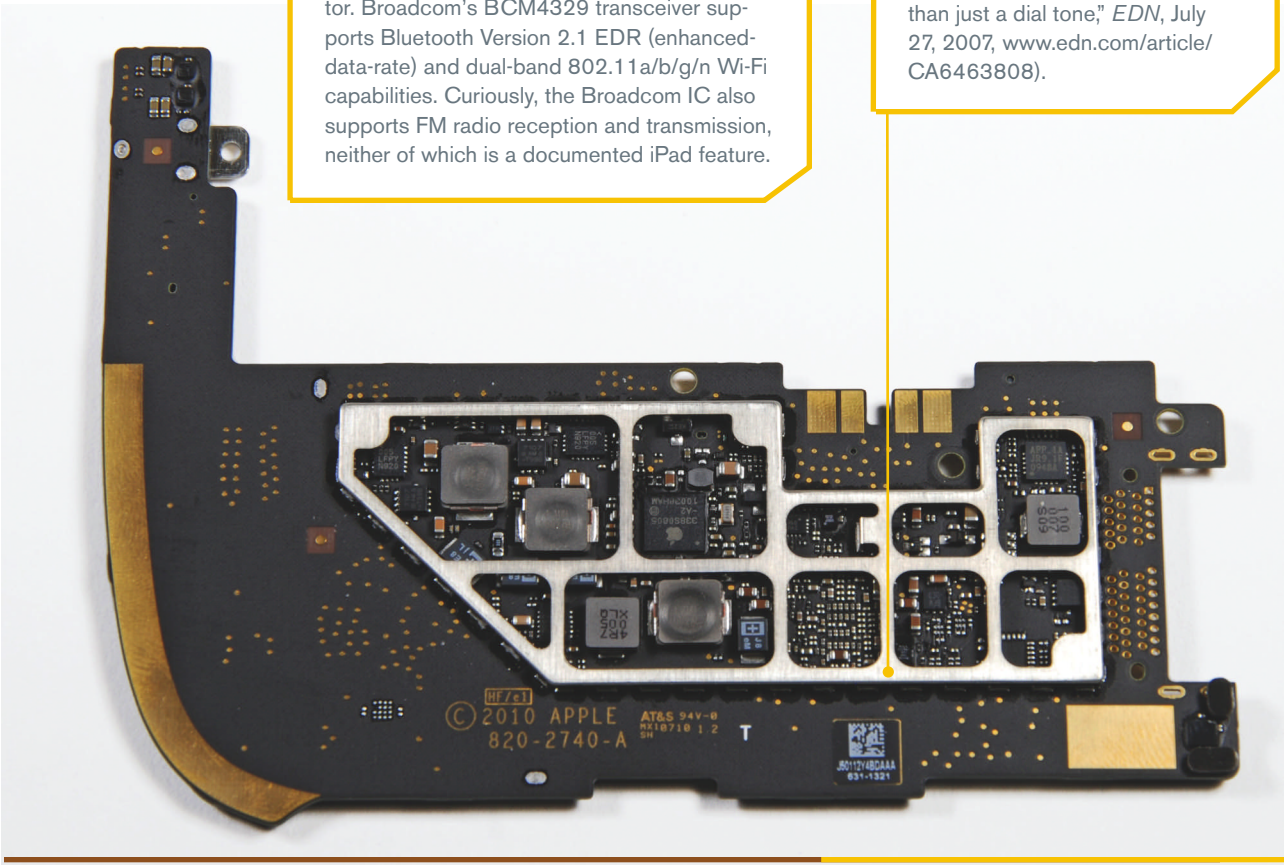
This particular iPad is a Wi-Fi-only unit, lacking the 3G (third-generation) UMTS (Universal Mobile Telecommunications System) HSPA (high-speed-packet-access) cellular-data capabilities found in more expensive iPad versions. As such, you won't find relevant ICs, which mount on an add-in module in one corner of the unit. These ICs include Infineon's PMB 8878 X-Gold baseband chip and PMB 6952 dual-mode RF transceiver; Skyworks' Sky77340 power-amplifier module; Triquint's TQM616035A, TQM666032B, and TQM676031A power-amplifier/filter combinations; Numonyx's 36MY1EE NOR-flash memory containing additional system firmware; and Broadcom's BCM4750 implementing the A-GPS (assisted global-positioning-system) function that's also unique to the cellular-cognizant iPad.



The discrete wireless-communications module resides on the cable that interconnects the primary PCB and the bottom-edge dock connector. Broadcom's BCM4329 transceiver supports Bluetooth Version 2.1 EDR (enhanced-data-rate) and dual-band 802.11a/b/g/n Wi-Fi capabilities. Curiously, the Broadcom IC also supports FM radio reception and transmission, neither of which is a documented iPad feature.

Nonvolatile memory on the iPad comprises two 64-Gbit MLC (multilevel-cell) NAND-flash-memory ICs for 16 Gbytes of total resident storage on the primary PCB's front side; 32- and 64-Gbyte iPad variants are also available. An 8-Mbit SPI (serial-peripheral-interface) flash-memory IC, presumably containing system boot code, resides on the PCB's backside. This iPad employs Samsung-sourced NAND devices, whereas the FCC (Federal Communications Commission) characterized a unit that used Toshiba-fabricated silicon. The Atmel-stored system-firmware selection mimics Apple's choice on the second-generation iPod touch (see "Studying the second-generation Apple iPod touch," *EDN*, Sept 30, 2008, www.edn.com/article/CA6600223) and marks a departure from the Intel IC on the first-generation iPhone (see "Inside Apple's iPhone: more than just a dial tone," *EDN*, July 27, 2007, www.edn.com/article/CA6463808).



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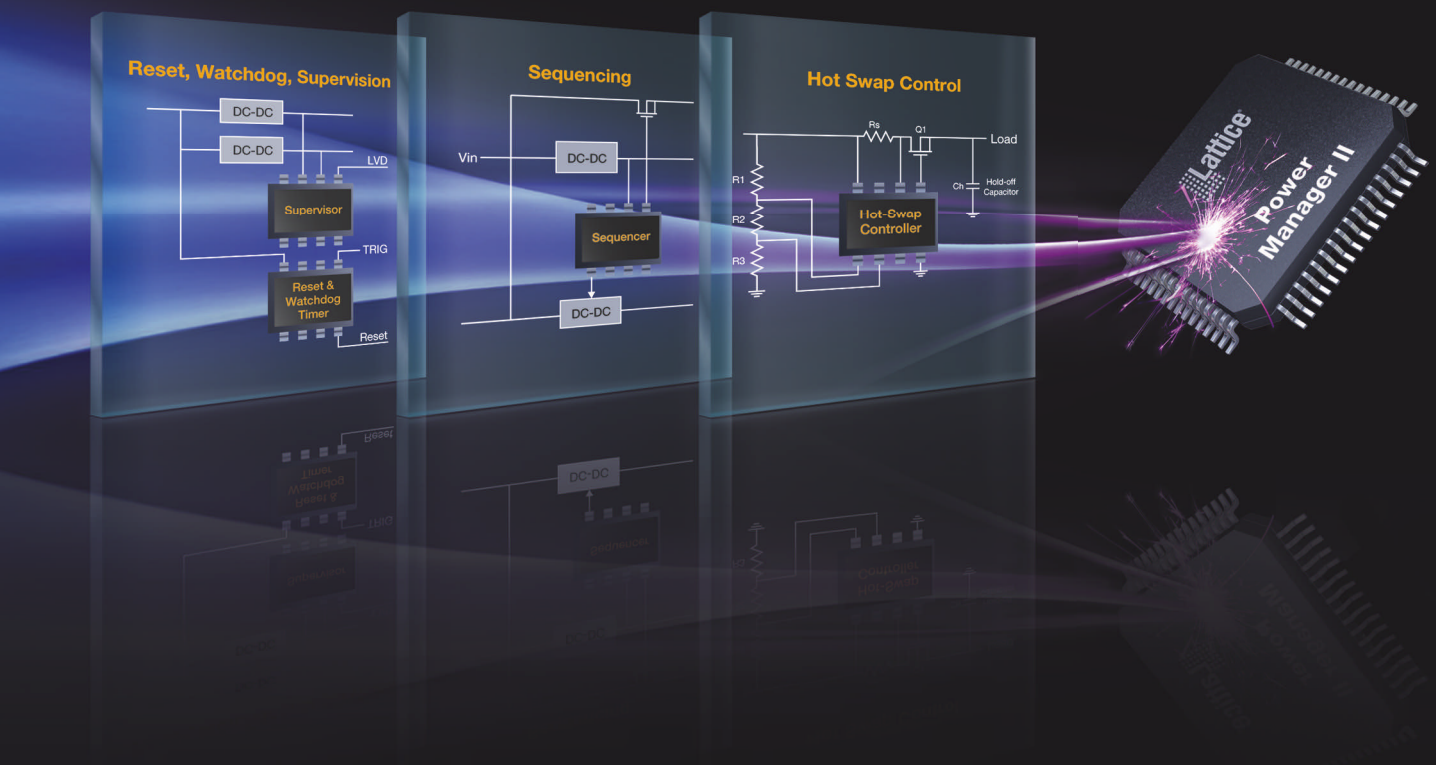

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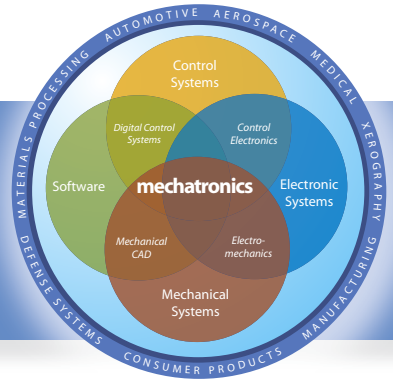
MECHATRONICS IN DESIGN

FRESH IDEAS ON INTEGRATING MECHANICAL SYSTEMS, ELECTRONICS, CONTROL SYSTEMS, AND SOFTWARE IN DESIGN



Handling the World Wide Web

Before the World Wide Web, engineers were handling webs at astonishing speeds.

The word "web" means different things to different people. To some, "web" conjures up images of Spider-Man, while most others may think of the ubiquitous World Wide Web. However, for many engineers, the word "web" brings to mind the pervasive and astonishing material web used in many processes that make the majority of the products we all use. Let's explore this overlooked material-handling application that is indispensable in so many diverse industries. And while we are doing that, let's ask the question, Why is there a gap and time lag between the latest technological advances in web handling and actual industrial practice, an observation not unique to this application?

Academic rigor and the best practices of industry need to be merged in an understandable, usable way for innovation to occur and result in tangible advances.

The economic advantage of manufacturing a material continuously instead of in batches is clear. The inputs and throughputs to continuous manufacturing processes are usually webs. A web is defined as a long, thin, flexible material with negligible bending stiffness about two of its three axes. Major classes of web materials include film, foil, food, paper, nonwovens, rubber, textiles, and composites of these. Materials range from centimeter-thick metals to micron-thick plastics; widths range from single, thin strands to more than 10m; and line speeds can reach more than 2,500m/min.

The goal of web handling is getting a web through a machine as fast as possible with minimum damage and waste, while preserving the web's properties. Web manufacturing forms the raw-material web (for example, paper making, film extrusion, textile spinning), while web converting (for example, coating, laminating, printing, sheeting) takes one or more web materials and permanently alters them in some fashion either by changing material properties or causing geometrical/physical changes. Web manufacturing and converting are often done by a combination of mostly art (trial and error) and a little bit of science, depending on the industry. However, all webs follow the same laws of physics—if we know the physics, we know the behavior. Web handling is an exact science with model-based design rules; all webs behave fundamentally the same way when pulled through a machine under tension. There even exists a wealth of literature and experts—D.H. Carlson, 3M Corp.; P.R. Pagilla, Oklahoma State University; and M.D. Weaver, Rockwell Automation—in this area. Monitoring and controlling web velocity and tension is a common web-handling challenge.

Kevin C Craig, PhD, is the Robert C Greenheck chair in engineering design and a professor of mechanical engineering, College of Engineering, Marquette University. For more mechatronic news, visit mechatronics zone.com.

The use of a model-based design approach, rather than a trial-and-error design approach, is fundamental in modern mechatronic system design. Why is this approach not more widespread when applied to webs? There is a gap, and time lag, between the academic and research world and the world of industrial practice. More than 10 years ago, Dennis Bernstein wrote an article in the *IEEE Control Systems Magazine* entitled "On Bridging the Theory/Practice Gap," in which he states that both sides contribute to the problem. The article was timely then and is even more so now.

So what needs to happen to bridge this gap? Academic rigor and industry best practices need to be merged in an understandable, usable way for innovation to occur and result in tangible advances. On the academic side, professors need to get out of their comfort zone and make each course, from freshman year through the graduate programs, an up-to-date fusing of academic rigor and best industrial practice with actual industry case studies as examples.

Too hard? Too challenging? This is what transformational engineering education is all about. On the industrial side, companies need to recognize that their competitive advantage comes from an inspired, educated workforce, and that should be their primary concern. Too often the training budget is the first to be cut, with the view that technological advances somehow arrive with the morning newspaper. Too harsh an assessment? I do not think so, and I do not believe the rest of the world thinks so either. EDN

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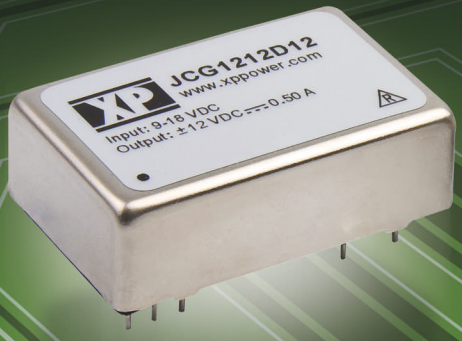

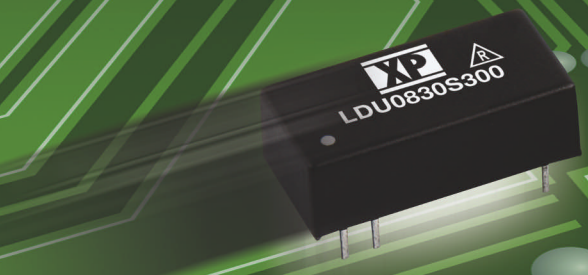

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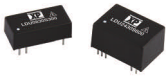

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RECONFIGURABLE SINGLE-CHIP RADIOS

BY JAN CRANINCKX AND PIET WAMBACQ • IMEC

In the future, mobile devices will have more and more access to all kinds of communications and multimedia services. They will have access not only to mobile-phone networks and the mobile Internet, but also to global-positioning systems, broadcasting services, WLAN (wireless-local-area-network) services, short-range connectivity, and many others. These future devices will also function in all kinds of situations—at home, in the office, during travel, and so on. ICs for these future mass-market wireless-communication consumer applications will be competitive only when they become small, energy-efficient, and cost-effective.

TERMINAL PERFORMANCE

Ideally, a single mobile terminal should be able to accommodate all the communications functions a consumer would want. To ensure that such a terminal is low-cost, it is essential to minimize the area or form factor of the IC that implements the necessary communications functions within the terminal. The only way to achieve that goal is through extreme IC integration because IC integration can add features to a chip without increasing its area. Moreover, the IC should thus not just be a single-chip multistandard radio but instead a flexible radio chip. The RF part should integrate with the digital part of the radio in a single-chip SOC (system on chip). The flexible radio chip should be software-reconfigurable over a large range of communication standards, and it should be able to do the same job as several separate single-mode radios.

Due to its flexibility, a software-defined radio would also enable the new mobile terminals to choose the best standard for each situation. As a result, its flexibility will enhance the quality of the service and will enable the terminal to optimize its energy efficiency.

Integrating the RF part of the radio with the digital part onto a single IC is one of the main challenges. Engineers must perform this integration in a digital-scaled nanometer technology, in which it is essential to minimize the area of the RF part. People commonly assume that analog circuits do not scale with technology, which could endanger the cost advantage.

Researchers at IMEC (Interuniversity MicroElectronics Center), however, along with its partners, have succeeded in solving this challenge. The researchers have proved that the scaling of the analog part is possible and have demonstrated this ability by realizing a high-performance, low-area, reconfigurable single-chip radio. The new chip is a 5-mm^2, flexible RF transceiver in 40-nm, low-power digital-CMOS technology (**Figure 1**). The chip exhibits RF performance that is comparable with that of state-of-the-art multiple-chip radios (**references 1** through **3**). To achieve this size and high performance, the company used the benefits of aggressively scaled low-power CMOS technology, such as the high intrinsic speed of the nanoscale transistors and less variability between the transistors. Engineers combined the use of the technology with a fundamental rethinking of radio-circuit architectures and designs to ensure that the analog-unfriendly nature of nanoscale technology would not degrade performance.

ANALOG CIRCUITS DO SCALE

On-chip capacitors provide examples of analog's ability to scale down. Earlier generations of capacitors needed expensive technology options to create MIM (metal-insulator-metal) capacitors, but nanoscale CMOS technology and the progression in lithography techniques and metal stacks have resulted in MOM (metal-oxide-metal) capacitors. These capacitors enable a much higher capacitor density. MOM capacitors are purely digital, meaning that they are free, along with the normal digital processing. Hence, in new CMOS nodes, analog circuits do partially scale down in area.

Moreover, the technology's matching parameters improve along with the progression in the processing techniques. The better transistor matching per area is another argument that analog circuits do scale. Analog circuits profit from better process control, which results in smaller transistors that are now more

identical to each other than were the transistors of 10 years ago. The result is a significant increase in the transistor density, minimizing the area and increasing the performance.

Analog's scaling benefits are limited, however. Therefore, most improvements in nanometer CMOS radio circuits must come from a fundamental rethinking of the front end's circuit and architectures. In this case, it is crucial to limit the large area penalty that is associated with the use of inductors for high-frequency operation. The best way to minimize the area would be to remove the inductors from the RF circuits. In some cases, you can now eliminate the use of inductors in the circuit design because the design uses 40-nm transistors. These nanoscale transistors have a much higher intrinsic speed than the transistors of larger nodes.

In other cases, you cannot eliminate the use of inductors because they are essential to maintaining the circuit's performance. In that case, you can minimize the area and maintain the circuit performance by designing circuit architectures using small inductors with a slightly lower quality. New low-noise amplifiers, for example, allow the use of low-Q inductors without degrading performance. Finally, in some cases, the use of inductors is unavoidable, as in, for example, VCOs (voltage-controlled oscillators). In this case, you can use circuit architectures that operate at higher frequency and that require smaller inductors and, hence, smaller area.

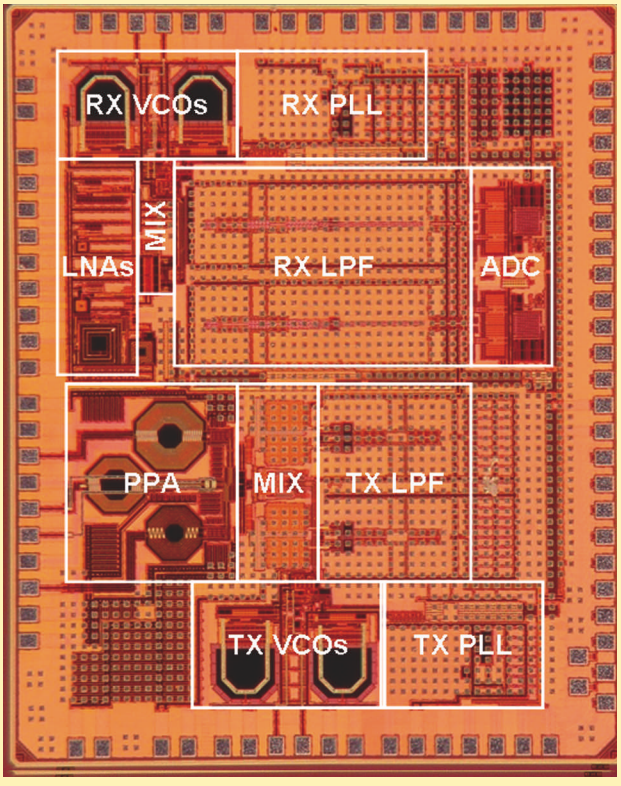
AT A GLANCE

- A flexible, cost-effective radio chip will integrate RF and digital parts.
- People often erroneously assumed that analog circuits do not scale.
- LP (low-power) CMOS technology and a fundamental rethinking of radio-circuit architectures yielded a flexible single-chip device.
- Purely digital MOM (metal-oxide-metal) capacitors enable high capacitor density.
- It is crucial to limit the area penalty associated with the use of inductors.

DIGITAL CONTROL

An equally important strategy for area limitation is the use of heavy digital control and digital compensation of the analog circuits. Whereas designers once used analog techniques to solve the variability in analog circuits, they can now use digital-control mechanisms. You use software to make the analog blocks digitally reconfigurable so that they can adapt themselves to the required performance and so that you can compensate for process variability.

You solve other analog imperfections that occur, such as mismatch and linearity errors, not by making the transistors larger but instead by using digital-signal processing—for example, by applying clever digital algorithms and calibration techniques. The transistors for this digital control are very small and thus involve practically no overhead cost with respect to area and power consumption.



ADC=ANALOG-TO-DIGITAL CONVERTER
LNA=LOW-NOISE AMPLIFIER
LPF=LOWPASS FILTER
MIX=MIXER
PLL=PHASE-LOCKED LOOP
PPA=PREPOWER AMPLIFIER
RX=RECEIVER
TX=TRANSMIT
VCO=VOLTAGE-CONTROLLED OSCILLATOR

Figure 1 This prototype of a 5-mm^2 flexible RF transceiver in 40-nm, low-power digital-CMOS technology demonstrates that you can achieve state-of-the-art RF performance in low-power digital-CMOS technology.

The realization of a high-performance, low-area reconfigurable single-chip radio is essential for future mobile terminals in which low-cost, low-area, and energy-efficient approaches will be necessary in wireless-communication applications for the high-volume consumer market. **EDN**

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2. Giannini, Vito, Pierluigi Nuzzo, Charlotte Soens, Kameswaran Vengattaramane, Julien Ryckaert, Michael Goffioul, Björn Debaillie, Jonathan Borremans, Joris Van Driessche, Jan Craninckx, and Mark Ingels, "A 2-mm^2 0.1- to 5-GHz Software-Defined Radio Receiver in 45-nm Digital CMOS," *IEEE Journal of Solid-State Circuits*, Volume 44, No. 12, December 2009, pg 3486.
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AUTHORS' BIOGRAPHIES

Jan Craninckx obtained his master's and doctoral degrees in microelectronics summa cum laude from the ESAT-MICAS laboratories of the Katholieke Universiteit Leuven in 1992 and 1997, respectively. His doctoral work was on the design of low-phase-noise CMOS-integrated VCOs and synthesizers. From 1997 to 2002, he worked with Alcatel Microelectronics (later part of STMicroelectronics) as a senior RF engineer on the integration of RF transceivers for GSM, DECT, Bluetooth, and WLAN. In 2002 he joined IMEC (Leuven, Belgium), where he currently is senior principal scientist in the analog-wireless research group. His research focuses on the design of RF-transceiver front ends for software-defined radio systems, covering all aspects of RF, analog, and data-converter design. Craninckx has authored and co-authored more than 70 papers and several book chapters and has published one book on analog- and RF-IC design. He holds 10 patents. He is the chairman of the SSCS Benelux chapter, is a member of the Technical Program Committee for both the ISSCC (International Solid-State Circuits Conference) and European Solid-State Circuits Conference, and is associate editor of the Journal of Solid-State Circuits.

Piet Wambacq, principal scientist at IMEC, received a master's degree in electrical engineering and a doctorate from the Katholieke Universiteit (Leuven, Belgium) in 1986 and 1996, respectively. Since 1996, he has been with IMEC (Leuven, Belgium), working as a principal scientist on RF-CMOS design for wireless applications. He is also a professor at the University of Brussels (Vrije Universiteit Brussel). Wambacq has authored or co-authored two books and more than 150 papers. He was an associate editor of the IEEE Transactions on Circuits and Systems *from 2002 to 2004. He is the co-recipient of the Best Paper Award at the DATE (Design, Automation, and Test Conference) in 2002 and 2005. He is also a member of the program committee of the European Solid-State Circuits Conference.*

IMEC ADDRESSED EUV AND NEUROELECTRONICS IN 2009

Nanotechnology research center IMEC (Interuniversity MicroElectronics Center) announced at its General Assembly meeting on April 30 that 2009 had been a satisfying year, with IMEC's total revenue amounting to €275 million, including €222 million coming from collaboration with the global industry. In addition, the Flemish government granted IMEC €44.7 million, and the Dutch government granted €8 million to IMEC the Netherlands at the Holst Centre.

In addition to its work with "green" radios, IMEC has been focusing on EUV (extreme-ultraviolet) lithography. The organization reports that it last year employed EUV lithography to fabricate the first functional 22-nm SRAM cell.

IMEC also took advantage of continuing transistor scaling to address new nanoelectronics and neuroelectronics applications. In 2009, the organization developed a micronail chip, which can make intimate contact with neurons, enabling it to stimulate neurons and read their signals. Researchers associated with the Neuroelectronics Research Flanders initiative (www.nerf.be) will use the chip to help unravel the secrets of the human brain. In addition, in 2009, IMEC successfully launched its solar-cell research program, in collaboration with companies such as Schott Solar, Total, GDF Suez, and Photovoltech.

IMEC's said its headcount exceeds 1750, including more than 550 industrial residents and guest researchers. It produced more than 1750 conference papers and publications during the year, often in collaboration with universities worldwide.

"Innovative organizations are in constant movement," says Luc Van den hove, president and chief executive officer of the center. "IMEC is no exception to that [trend]. In 2009, we worked hard to combine the strengths of our diverse expertise, independent of the location where research is performed. More and more innovation depends on combining knowledge in diverse disciplines," including technology, design, applications, and packaging. Van den hove adds, "This is our way to prepare for the future [and] to tackle the technological and the economical challenges ahead because we are convinced that open innovation and global collaborations are the key to progress."

BY MARGERY CONNER, TECHNICAL EDITOR

WHERE ARE YOU? WHO ARE YOU? WHAT ARE YOU DOING? ASSUME THAT SOMEONE OR SOMETHING—AN INDIVIDUAL, A COMPANY, OR A GOVERNMENT—KNOWS THE ANSWER TO ALL OF THESE QUESTIONS. IS THIS SCENARIO A NIGHTMARE OR THE NEXT OBVIOUS STEP TO DEFINING INDIVIDUALS IN OUR SOCIETY? WELCOME TO THE "INTERNET OF THINGS."

Sensors empower the "INTERNET OF THINGS"

THE "INTERNET OF THINGS" IS THE NETWORKED interconnection of objects—from the sophisticated to the mundane—through identifiers such as sensors, RFID (radio-frequency-identification) tags, and IP (Internet Protocol) addresses. Ford's Tool Link system, for example, builds sensors into vehicles, including the Ford Transit Connect, so that when the driver presses a button, the dashboard displays an inventory of all onboard tools. A similar system for homes would show you an inventory of all clothes that are supposedly in your suitcase or objects in your briefcase.

Sensors form the edge of the electronics ecosystem, in which the physical world interacts with computers, providing a richer array of data than is available from keyboards and mouse inputs. Currently, someone at a keyboard has input most of the information on the Internet. We are at an inflection point, however, at which more Internet data originates through sensors than keyboards.

The goals for the Internet of Things are, first, to instrument and interconnect all things and, second, to ensure that all those things are intelligent. Recall that the Bay Bridge linking San Francisco and Oakland, CA, had to close for several days last October after metal pieces fell onto the roadway. This scenario would likely not have happened in a world shaped by the Internet of Things. Instead, thousands of accelerometers on the bridge would have registered the vibratory signature of impending failure. A bridge the size of the Bay Bridge might have 10,000 sensors; a small overpass, 100.

COURTESY ELECTRICFOXY.COM, PHOTOGRAPHER: PETER GAAN

Combining the number of infrastructure sensors with the number of sensors in personal devices, such as cell phones, yields a round number of 1000 sensors per person that manufacturers will develop and deploy over the next 10 years. With a world population in the billions, this figure would translate to more than 1 trillion sensors. That many sensors collecting data implies a lot of data manipulation, which in turn implies a computing cloud—that is, the use of large numbers of computers, often over distributed data centers, to seamlessly process and store large amounts of data. At a typical data rate, 1 million sensors running 24 hours a day would require 50 hard disks running in parallel to capture the 20 petabytes of data these sensors would create in just six months. Companies that are already deep into cloud computing are jumping into the Internet of Things as a significant new business opportunity for their expertise. Two notable examples are IBM, with its Smarter Planet program, and Hewlett-Packard, with its CENSE (Central Nervous System for the Earth).

AT A GLANCE

- The "Internet of Things" will rely on sensors as data inputs.
- As many as a trillion or more sensor nodes will instrument much of our environment.
- Sensor networks will use a mixture of formal networks and ad hoc network architectures.

HP is using its MEMS (microelectromechanical) expertise, which it developed to provide fluid sensors for printer cartridges, to create accelerometers that are as much as 1000 times more sensitive than today's commercial products. The tiny MEMS accelerometers are the first CENSE sensors; follow-up sensors will include devices for light, temperature, barometric pressure, airflow, and humidity.

The first units to enter the field can detect a 10-femtometer positional change—less than 1-billionth the width of a human hair—measuring acceleration changes in the micro-g range. These abilities make the units approximately 1000 times more sensitive than the consumer-grade accelerometers that a Wii, an iPhone, or an automobile's airbag system currently uses (**Figure 1**).

Apart from the cost of the overall computing network, the sensors themselves, especially 1 trillion of them, represent a significant investment in infrastructure. Peter Hartwell, senior researcher for information and quantum systems at HP Laboratories, believes that the only way for large-scale sensor networks to become economically viable is to increase productivity and efficiency, thereby offsetting the cost of the network: "Look at the silicon that's embedded in a ski pass, for example. There's no deposit for that chip; it's literally free because the value it adds in replacing a lift operator [means that] the resort can afford to give away the [chips in the] passes for free." Networked sensors add value that will more than offset their costs, he says.

Although the cost of large-volume silicon hardware does tend toward zero over time, there's more to a sensor node than the silicon. Wireless-sensor nodes have four general components: the sen-

sor and its signal-conditioning circuit, the microcontroller, a radio transceiver, and a power source. The first three components benefit from Moore's Law and rapidly grow in capability while dropping in price. However, the power source doesn't rely on silicon integration and receives no such benefit. Whereas batteries, supercapacitors, and energy-harvesting devices have seen significant improvement over the past several years, energy storage and harvesting do not in general benefit from economies of scale. The power available is still about the same with a fixed budget on the order of milliwatts. The rest of the sensor nodes can now do more with that fixed power budget, however. Nonetheless, dedicated wireless-sensor nodes—for the near term at least—will have a formidable price hurdle to overcome.

Giant corporations such as HP and IBM are not the only pathway into the Internet of Things. For example,

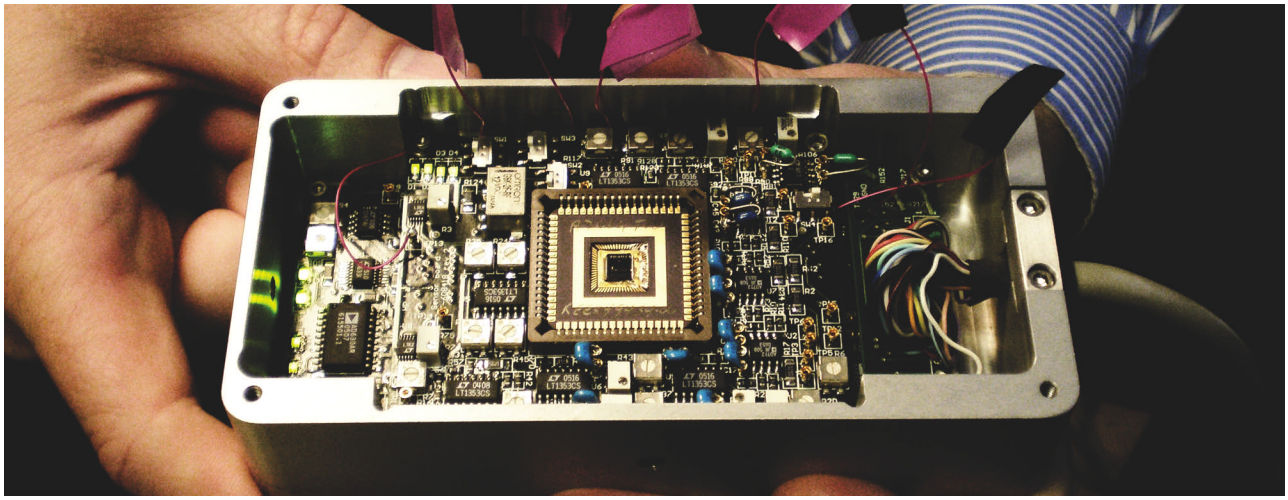

Figure 1 Wireless-sensor nodes, such as this one using an HP digital accelerometer, must shrink in size and cost to enable a trillion-sensor Internet of Things.

Pachube, an open-source-based private company, allows creators and users with automatically generated sensor data to upload it to the Pachube site for the Pachube community's use. Pachube's generalized data-brokering platform is a way for small companies and researchers whose expertise lies in developing products, rather than networking, processing, and storing data, to access the Internet of Things (**Reference 1**).

In addition, the Internet of Things isn't restricted to fixed, formal network architectures. Ad hoc sensor networks can also form around personal mobile-communication devices. If you have a smartphone in your pocket, purse, or backpack, you're carrying a variety of sensors. For example, the iPhone senses location, motion, direction, sound, and images through its GPS (global-positioning system), accelerometer, digital compass, microphone, and camera, making you a walking sensor node (**Reference 2**).

Smartphones can communicate with other users, sending location and sensor information. The information can be as simple and local as "Where are you?" for parental monitoring of a teen's whereabouts, or it can be more complex. "Real network power may come when fixed formal networks can link up with ad hoc networks," says HP's Hartwell. "For example, speed and location data from mobile phones can mesh with smart highway sensors."

Figure 2 This prototype hoodie has a built-in wireless-communication interface that alerts wearers when their Facebook pages have changed and allows quick gestural Facebook responses, rather than relying on keyboards (courtesy electricfoxy.com, photographer: Peter Gaan).

Figure 3 Disney Cruise Lines outfitted some of its interior windowless staterooms with round flat-panel screens that display a video of exterior scenes. The porthole can sense when people are present and display interactive Disney characters. As a result, the rooms command premium prices.

The preponderance of mobile devices grooms humans to better support systems for sensors, training us to make sure our cell phones and mobile devices are well-charged; otherwise, we can't talk or entertain ourselves with music and videos. Wireless headsets introduce another power source. If you want to monitor a person's physical state, there are few better places to put a sensor network than on your head, and Bluetooth headsets introduce another battery, which you must frequently charge, right on your head. We as consumers are enabling the power environment for human-based sensor networks.

Ping, a prototype hoodie with a wireless interface, alerts wearers when their Facebook pages have changed and allows quick gestural Facebook responses (**Figure 2** and **Reference 3**). Keyboard-avoiding Facebook users are probably not such a huge market that they will define input/output design for portable devices, but they do represent a growing need to monitor and react to people who may not be well-behaved I/O devices for computers. An example of this growing market is the elderly. Full-time care for elderly patients who are at risk of falling is expensive, and, from an independent-minded patient's point of view, not necessarily desirable. Wearing an accelerometer-equipped, wireless node that sends an alert when it senses a fall can be a substitute for full-time personal care.

For some patients, adjusting their environment itself may be part of their treatment. Speaking at *EDN*'s March 2010 Designing with LEDs Workshop, Cary Eskow, director of Lightspeed, explained that light in the blue spectrum affects our alertness and attitude, so there are times during the day in an elderly-patient-care facility when blue light is appropriate for some patients. Rather than periodically wheeling patients to the Blue Room, a sensor-driven lighting network can adjust a room's light color—but only when the appropriate patient is present. For this scenario to happen, the room must sense which patients are present and adjust the light for the time of day.

Electronic health records will play an increasingly important role in future health care and health-care costs. These records currently rely on manual input,

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limiting the accuracy and amount of data someone enters. Accessing patient information, including identification and vital signs, directly from sensors will correct both problems. Again, however, the sensors must be networked for real-time feedback. Just as important, sensor-based patient monitors can help in understanding disease. Rather than relying on patients to fill out questionnaires about their health history and habits, sensors will do it more accurately and more often. Networked medical information that combines results from thousands or millions of subjects will point out problems and suggest possible methods of treatment.

The full-blown, networked system of a trillion sensors is probably at least 10 years away, but an example of a smaller sensor network would be within buildings, ranging from private homes to commercial buildings of millions of square feet. Networked, or "smart," buildings automatically dim or turn off lights when people leave and adjust energy use based on occupation. The focus of smart homes or smart buildings is energy efficiency, but these networks all rely on a network of sensors to determine people's usage in concert with environmental effects, such as temperature, humidity, and time of day.

Redwood Systems uses Ethernet, ubiquitous in most commercial buildings, to both power and control its buildings' lighting, but the network is not limited to lighting management. Brent Boekenstein, director of business development, refers to Redwood's network system as a rich sensor network in ceilings, enabling every light bulb to have both a sensor and an IP address. He uses as an example one company in a humid Asian environment that had a problem with mold in the ceiling. The company added a mold sensor into the building's lighting platform. Redwood's platform can work with both LED and fluorescent lights.

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LED lighting is a good example of how sensors and the Internet of Things can increase the value of an environment. LED lights, although efficient, are not significantly more efficient than fluorescent lights in many applications, and they are significantly more expensive. However, LEDs have additional functions, such as dimmable light intensity and color control. Disney Cruise Lines has fitted its less-desirable interior, windowless staterooms with round flat-panel screens, or "virtual portholes," which display a live video of the outside environment (**Figure 3**). The porthole can sense when people are present and superimpose interactive Disney characters; as a result, the rooms command a premium price. Add LED lighting to the light network, and a room with virtual windows can mimic outdoor lighting, complete with dimming on overcast days and day-to-night light cycling.

In a world in which common objects have their own IP address and your cell phone might be talking to them, privacy is a significant concern. "Congratulations! You made my list of supervillains," commented an online news article after HP announced CENSE. HP's Hartwell argues, however, that the Internet of Things could develop a sensor network that ensures that the data is valid and still maintain anonymity. **EDN**

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Power management for optimal power design

A HOLISTIC APPROACH TO POWER MANAGEMENT, FROM TRANSISTORS TO FULL-CHIP TECHNIQUES, IS NECESSARY FOR MEETING TODAY'S POWER-MANAGEMENT GOALS.

Optimization of power consumption is one of the biggest challenges IC designers face today. Although power optimization has always been critical for battery-operated designs, the continued growth of system performance with each new generation of semiconductor technology, along with the increasing emphasis on "green" and "clean" technical applications, has made power optimization essential even for wall-powered designs. Effective power management involves selection of the right technology, the use of optimized libraries and IP (intellectual property), and design methodology (**Figure 1**). It also means optimizing both active dynamic power and static leakage power. This article examines the various approaches to effective power management.

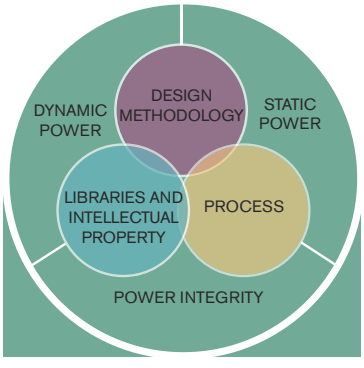


Figure 1 Effective power management requires proper technology selection, library and IP design, and chip-design methods.

Power consumption is becoming more important in electronics. With increasing emphasis on reducing energy consumption in products, system designers must take more care in managing their power budgets. As a result, managers slash chip power budgets and maintain cost and performance goals. Unfortunately, the migration to finer technologies is compounding the problem. First, leakage power increases significantly with finer geometries and is becoming a key component of the total power. In addition, the finer geometries do not provide the voltage scaling that previous generations of technology enjoyed. As a result, the power saving due to voltage scaling is no longer substantial. In addition, from a design perspective, chips in the new generation of technology normally see a major increase in features and functions. Taking all these factors into account makes power management a significant challenge for most designers. So designers need an intelligent approach for optimizing power consumptions in designs.

BASIC OPERATION OF MOS TRANSISTORS

To understand power, begin with the classic MOS-transistor equations for the drain current. Although these equations are accurate only for older technologies and do not take into account various effects that the submicron geometries in modern technologies introduce, they provide an understanding of the overall behavior of the transistor.

In digital circuits, when the transistor is on, it is in the saturation region, in which the following equation governs the drain-to-source current, I_{DS} (**Figure 2**):

$$I_{DS} = K\frac{1}{T_{OX}}\frac{W}{L}(V_{GS}-V_{TH})^2, \quad (1)$$

where T_{OX} is the gate-oxide thickness, W is the channel width of the transistor, L is the channel length of the transistor, V_{GS} is the voltage between the gate and the source of the transistor, V_{TH} is the threshold voltage, and K is dependent on the process technology. The following equation governs the threshold voltage:

$$V_{TH} = V_{FB} + \Theta_S + \gamma\sqrt{V_{SB} + \Theta_S}, \quad (2)$$

where V_{SB} is the back-bias voltage between the source and the substrate; V_{FB} is the flat-band voltage, which depends on the process technology; and γ and Θ_S are parameters that also depend on the process technology.

If the drain-to-drain voltage is the power-supply voltage—that is, the maximum voltage that can be between the gate and the source, you can use the following equation to calculate the on current:

$$I_{ON} = K\frac{1}{T_{OX}}\frac{W}{L}(V_{DD}-V_{TH})^2. \quad (3)$$

You can then express the active power as:

$$P_{ACTIVE} = I_{ON}V_{DD} = K\frac{1}{T_{OX}}\frac{W}{L}(V_{DD}-V_{TH})^2 V_{DD}. \quad (4)$$

LEAKAGE POWER

The main components of leakage in a MOS transistor are junction leakage, gate leakage, gate-induced gate leakage, and subthreshold conduction. Junction leakage occurs when the PN junction between the drain and the substrate or the source and the substrate becomes negatively biased when the transistor is off, resulting in a leakage current due to the presence of the reverse-bias diode. Gate leakage occurs in the presence of a high electric field in the gate oxide, causing electrons to tunnel through the gate into the substrate and resulting in gate leakage. As transistor geometries shrink, the gate-oxide thickness also decreases, making it more prone to tunneling. However, new high-k dielectric materials for the gate oxide have managed to control and minimize this leakage.

Gate-induced drain leakage occurs when the high electric

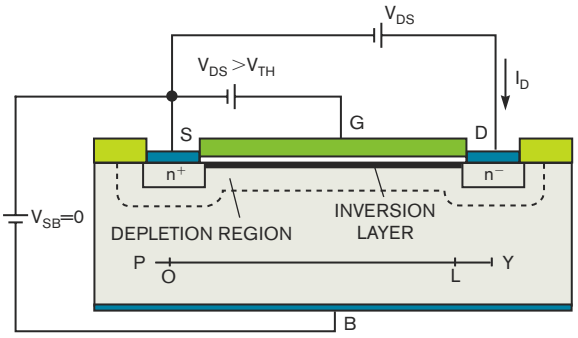


Figure 2 An NMOS FET shows the voltages you apply at its terminals.

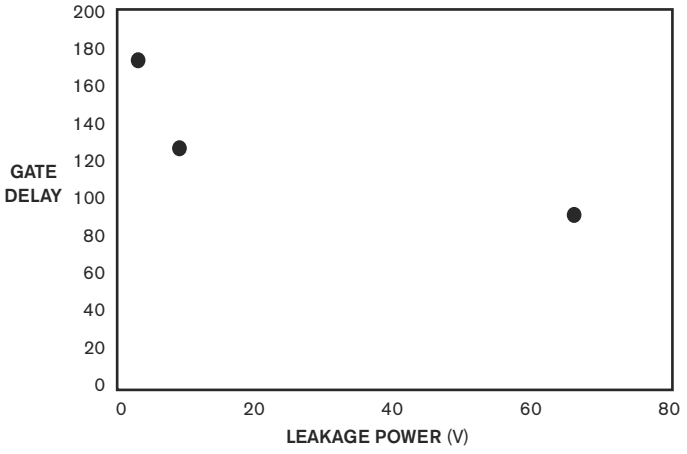


Figure 3 There is a trade-off between leakage and power.

fields in the gate-to-drain overlap region cause band-to-band tunneling and result in gate-induced drain-leakage current. Subthreshold conduction occurs when the transistor is off; it is not truly off but conducts due to weak inversion. Subthreshold conduction is the main contributor of leakage current. You can express this current as:

$$I_{DS}=K_1\frac{W}{L}\exp\left(\frac{V_{GS}-V_{TH}-\gamma V_{SB}+\eta V_{DS}}{NV_T}\right)\left(1-\exp\left(\frac{-V_{DS}}{V_T}\right)\right), \quad (5)$$

where K_1, γ, η, and N are technology-dependent, V_T is the thermal voltage, and K_1 is a function of the gate-oxide thickness. You can obtain the off current or leakage current in a transistor by setting the gate-to-source voltage at 0V and setting the drain-to-source voltage to equal the power-supply voltage, V_{DD}. Under these conditions, you can approximate the term

$$1-\exp\left(\frac{-V_{DD}}{V_T}\right) \quad (6)$$

to 1 because the power-supply voltage is much greater than the thermal voltage, leading to

$$I_{OFF}=K_1\frac{W}{L}\exp\left(\frac{-V_{TH}-\gamma V_{SB}+\eta V_{DD}}{NV_T}\right). \quad (7)$$

You can now write the leakage power as

$$P_{LEAKAGE}=I_{OFF}V_{DD}=K_1\frac{W}{L}\exp\left(\frac{-V_{TH}-\gamma V_{SB}+\eta V_{DD}}{NV_T}\right)V_{DD}. \quad (8)$$

From this result, you can see that the main parameters controlling the power are the threshold voltage, the oxide thickness, the transistor length and width, the power-supply voltage, and the back-gate bias. Because active power varies as the square of the power-supply voltage, reducing the power-supply voltage has the most impact on reducing active power. The reduction in power is twice the amount of reduction in voltage—that is, a 20% reduction in power-supply voltage yields a 40% reduction in active power. The remaining parameters affect active power only linearly. Any significant change in length, width, or threshold voltage has adverse effects on the performance of the transistor. As a result, designers can change these parameters only by small amounts, and they therefore have only a small role on reducing active power. However, they do have a significant impact in reducing leakage power because they are exponentially related to it. From **Equation 5**, you can see that

$$\frac{I_{DS}(V_{GS}+\Delta V_{GS})}{I_{DS}(V_{GS})}=\exp\left(\frac{\Delta V_{GS}}{NV_T}\right). \quad (9)$$

If $\Delta V_{GS}=-NV_T$, the equation becomes

$$\frac{I_{DS}(V_{GS}+NV_T)}{I_{DS}(V_{GS})}=\frac{1}{e}, \quad (10)$$

meaning that the subthreshold current decreases by a factor of 2.71828 for every NV_T reduction in effective gate-to-source voltage. N is typically 1 to 2.5 for a technology, and the threshold voltage is 26 mV at room temperature, so, for every 50- to 75-mV change in gate-to-source voltage, you can see a reduction of 2.7 in subthreshold current. Increasing the threshold voltage has the same effect. Thus, for every 50- to 75-mV increase in threshold voltage, the leakage current decreases by a factor of 2.7. A 100- to 150-mV increase in threshold voltage reduces leakage by a factor of 7.4.

You can further reduce leakage current by increasing the back-gate bias. The gain is less significant due to the presence of the body-bias coefficient, γ. Reducing the power-supply voltage also helps to reduce leakage current. Increasing the channel length of the transistor not only directly reduces leakage current, as in **Equation 5**, but also helps to increase the threshold voltage, as in **Equation 2**.

The subthreshold current has an exponential dependence on temperature. Because the term NV_T appears in the denominator of the negative exponent, as the temperature increases, the current increases significantly. This increase poses a major challenge because leakage power becomes a significant component of total power at high temperatures. So you must consider the total power at high temperature for fast-process-corner devices for worst-case power analysis.

Now that you understand the parameters that affect active and leakage power, you should examine how you can control these parameters using process-technology and design methods.

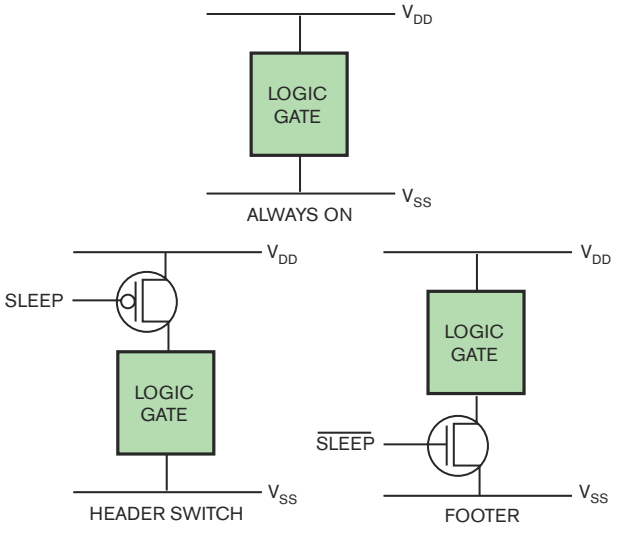


Figure 4 You can use header and footer switches to turn off logic to save active power.

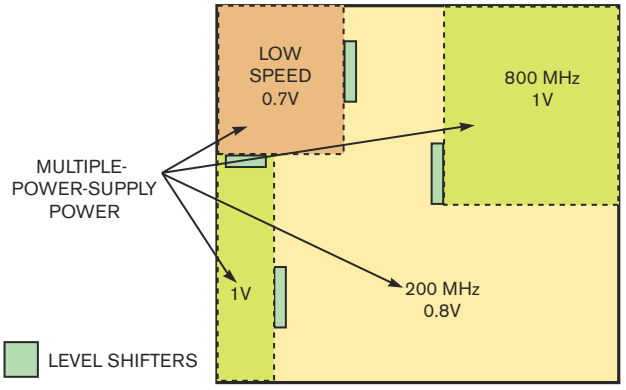


Figure 5 In a chip with multiple power domains, the low-performance portions use lower-power supplies to reduce power. Level shifters properly interface the logic in the different domains.

THE ROLE OF TECHNOLOGY SELECTION

Proper technology selection is one of the key aspects of power management. The goal of each technological advancement is to improve performance, density, and power consumption. The typical approach in developing a new generation of technology is to apply constant-electric-field scaling. Process designers scale both the applied voltage and the oxide thickness to maintain the same electric field. This approach reduces power by about 50% with every new technology node. However, as the voltage gets smaller, the threshold voltage also must scale down to meet the performance targets of that technology. This scaling unfortunately increases the subthreshold current and hence the leakage power. To overcome this constraint, process engineers no longer apply constant-field scaling for processes of 65 nm or smaller; instead, they used a more generalized form of scaling.

Because it is impossible to optimize a technology for both performance and leakage at once, each technology usually has two variants. One variant aims for high performance, and the other shoots for low leakage. The primary differences between the two are in the oxide thickness, supply voltage, and threshold voltage. The technology variant with the thicker gate oxide aims for low-leakage design and must support a higher voltage to achieve a reasonable performance.

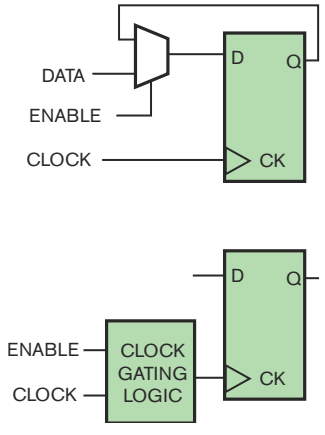


Figure 6 Clock gating eliminates the clock activity in a flip-flop during cycles when its input is inactive.

Equation 2 shows technology-dependent parameters γ and Θ_S, which you can manipulate to control the threshold voltage. These parameters depend on the doping concentration, which process designers can adjust by using an additional implant mask. This adjustment allows you to use one technology to create devices with multiple threshold voltages. You can then use this method to control leakage power in your designs.

When selecting a technology to optimize the power for a given design, you must take both aspects into consideration: the need to use a smaller geometry to reduce active power and the need to use a low-leakage variant to reduce leakage. There is a trade-off, however, with cost and risk.

Smaller geometries require a higher initial investment in mask costs and other NRE (nonrecurring-engineering) expenditures. Although they provide an advantage in unit cost because more units are available per wafer, they also pose a higher risk in process and design maturity. The design risk can be high if the design contains complex circuits such as SERDES (serializers/deserializers) or other sensitive blocks that are new in that process. The process risk depends on how long the technology has been in full production at the foundry. A new technology usually takes a year or more of production to iron out all the process kinks and to provide stable yields.

Should you aim for high performance or low leakage, and which is suitable for optimizing power? The answer to this question depends on both the nature of the power and the end application. If the end application is battery-powered, then you must minimize leakage. This constraint might automatically lead you to select a low-leakage technology, but that scenario need not always occur. For example, if you can turn off the design in standby mode, your design doesn't need a low-leakage process because you can turn off circuits in a high-performance system and also achieve the benefits of low leakage.

Low-leakage processes also use higher voltages and typically have larger areas and therefore consume more active power for the same performance. Leakage power is therefore the primary driver of the selection of a low-leakage process. Selecting a low-leakage process meets the requirements when leakage power becomes a significant component of the total power in a design during its active operation or when a design has a stringent requirement for the power in the standby mode that leakage dominates. In most other situations, you may select

the standard process along with a variety of circuit-design techniques to optimize power.

CIRCUIT-DESIGN TECHNIQUES

Once you select a technology, you can focus on the design techniques with which to optimize power. Start with the basic building block in a digital circuit: the logic gate. Logic gates are typically parts of a standard cell library. Each gate in a standard cell library uses the smallest transistors. Each type of gate has multiple versions with different drive strengths that employ wider transistors or multiple stages for more drive current. Because the main parameter for controlling active power is the power-supply voltage, cell designers typically design and characterize the gates to operate at voltages as much as 30% lower than the power-supply voltage. This voltage has performance implications. Lowering the power-supply voltage produces smaller currents, resulting in a longer time for charging and discharging the same capacitance. As a result, the design gets slower. However, this slowdown is acceptable if the design is not pushing the edges of a given technology.

Increasing the threshold voltage reduces the leakage current in the device. You can control leakage power by designing logic gates with multiple-threshold-voltage devices, including standard-, high-, and low-threshold-voltage devices. It is now common practice to design standard cell libraries with multiple-voltage-threshold devices. There is a trade-off between leakage and performance for a NAND gate that you implement with standard-, high-, and low-threshold-voltage devices (**Figure 3**). You can mix cells from these threshold-voltage libraries to optimize power in a chip.

The next factor is channel length. Cell designers create the logic gates in a standard cell library with minimum-channel-length devices. By increasing the channel length, you can reduce the leakage current in the device, but doing so also reduces the on current in the transistor and slows it down, so you can do this task only in small increments. Standard-cell-library providers recently created standard cells with multiple channel lengths. A combination of multiple-threshold-voltage devices and multiple channel lengths provides a rich standard-cell library for power management.

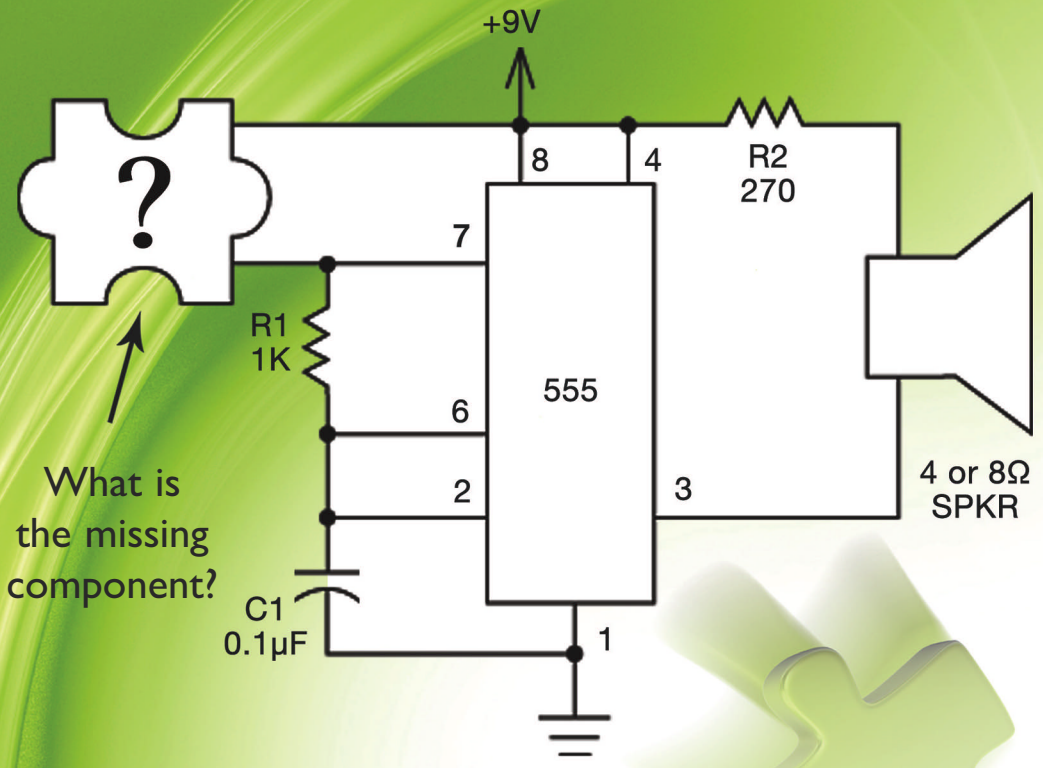
Another technique is back biasing. Traditionally, digital designers have viewed a MOS transistor as a three-terminal device in which the substrate ties to the source. As a result, the back-bias voltage is always 0V. By making the substrate available as a separate terminal and applying a reverse bias, you can increase the threshold voltage and lower leakage. You connect N-channel device substrates to a high negative voltage and P-channel device substrates to a high positive voltage. You need a large voltage for a small change in threshold because of the square-root relationship of the back-bias voltage to the threshold voltage as well as the presence of the body bias coefficient, γ. However, you apply back bias only in standby mode so that you don't affect the performance of the device.

The same techniques also apply to memory design. Memories can have high-threshold-voltage devices in both their bit cells and their peripheral circuitry as well as reverse-bias control to manage leakage in the off state. Using different combinations of threshold-voltage devices for the bit cell and peripheral circuitry provides extensive control of memory leakage and various levels of performance. Lowering the supply voltage in memories has a significant performance penalty. For this reason, memories typically require dual power supplies—a higher voltage for the bit cell and a lower voltage for the peripheral circuitry.

POWER MANAGEMENT

After examining power-management techniques at the circuit level, you can look at techniques at the chip level. The first is the use of power switches to shut down circuits when they are not in operation. In shutdown mode, the circuit consumes only leakage power and consumes no active power. You can further reduce leakage-power consumption by applying a back-gate bias. You shut down power by using MOSFETs as switches that connect to the power supply and ground rails (**Figure 4**). When implementing shutdown, you must consider how the circuit wakes up and you must sometimes preserve the state of the design. In this case, you can use reten-

Can You Guess the Missing Component?



Amateur electronic musician Joe Rhythm is planning a one-man video concert that he plans to post on YouTube. Controlling his array of instruments requires both hands and he wants to build a pressure-sensitive tone generator that he can control with a free finger or even an elbow or foot. Joe quickly whipped up a simple tone generator using parts from his bench stock. Since there wasn't enough time to order a pressure sensor, he improvised by making one from materials he had on hand. What did he use? Go to www.Jameco.com/brain6 to see if you are correct and while you are there, sign-up for our free full-color catalog.

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tion flip-flops to store the state. These flip-flops remain on in the shutdown state so that they can recover the state of the circuit when it wakes up. There is a small penalty in the form of wake-up recovery time.

You can use power switches to provide multiple levels of granularity in controlling which parts of the design need to shut down. You can switch power at the gate level, accompanying each gate by header and footer switches that connect to the power supplies. Alternatively, you can use header and footer switches with clusters of logic or at the block level with power islands. You can also use power islands without power switches by simply connecting the islands to different power supplies, which the design then turns on or off externally. These power supplies can have the same or different values. Power islands require the use of isolation cells at their boundaries. These cells ensure that the inputs to the island that is shut down are also off, so that there are no spurious currents.

A multiple-power-supply design has power islands with different values (**Figure 5**). This technique allows slower blocks of logic to run at lower voltages, thereby saving power. For multiple-power-supply designs, you must insert level-shifter cells at the island boundaries. These cells translate the logic into the appropriate levels of the island to which they interface. The UPF (Unified Power Format) language enables chip designers to describe designs with power gating and multiple power supplies. It allows the definition of power-supply domains for multiple-power-supply operation. It also allows the definition of isolation cells, level shifters, and power-gating switches. CPF (Common Power Format), a similar language, has the same purpose. These languages are currently competing to become the standard for defining power management in designs.

Today's EDA tools effectively support these power-management techniques. They also provide additional power savings during implementation. Because the clock network and the flip-flops they drive consume a significant amount of power, you can achieve power savings by turning off clocks when you don't need them to be running—that is, gating the clocks. Clock gating eliminates the clock activity in a flip-flop during cycles when its input is inactive (**Figure 6**). Clock gating can achieve active-power savings of more than 30%.

You can also optimize power in clock-distribution networks. By using cloning techniques, you break up the clock tree into smaller sections, thereby reducing the total capacitance in the clock network and lowering its power. The physical-optimization process also takes power into account. Once you meet the timing constraints, physical optimization downsizes the gates in the noncritical paths to reduce power without affecting timing.

LEAKAGE OPTIMIZATION

The main approach for optimizing leakage power is the use of standard cell libraries with multiple-voltage-threshold devices. Many tools allow a designer to use multiple libraries during physical implementation and automatically select cells from the appropriate library to optimize leakage power and meet performance targets. However, use this feature carefully because a design's area can sometimes become larger. Higher-threshold-voltage cells are weak, so your design may need larger cells to meet timing. In a mixed-threshold-voltage design, 80% of the cells typically have high threshold voltages, and the remaining 20% have either standard or low threshold voltages. You should use low-threshold-voltage devices sparingly and only in areas in which performance is critical because they contribute to leakage current. You can combine multiple-channel-length libraries with multiple-threshold-voltage devices to provide additional flexibility.

Another possibility is to use the TSMC (Taiwan Semiconductor Manufacturing Co, www.tsmc.com) Power-Trim service, which varies the channel length of transistors in noncritical paths, virtually without affecting the layout of the design. The technique applies a bias to the polysilicon mask, which instructs the mask-making process to make adjustments to increase the effective channel length of the transistor. Power-Trim does this task as a postprocessing step during manufacturing, and it has the advantage of not affecting the design schedule.

Once the design has met its performance targets, Power-Trim uses software that Tela (www.tela-inc.com) acquired from Blaze DFM to analyze the design

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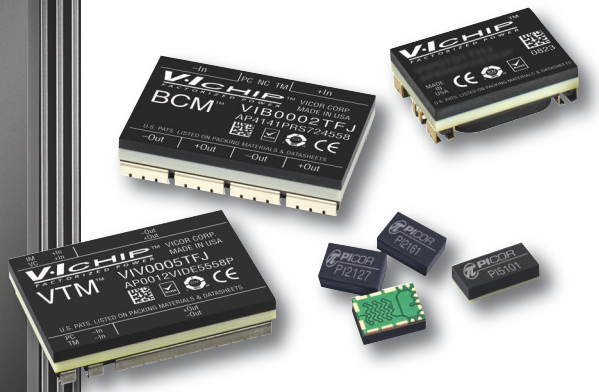

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and tag the transistors whose channel lengths could increase. Typically, these devices are in the noncritical paths of the design. The tool increases the channel lengths in predefined increments, which has a precharacterized standard-cell library. The tool performs a timing analysis with the modified gates to ensure that there is no impact on the chip's performance. This technique can provide an additional 20 to 30% savings in leakage power. Because this technique modifies only the transistors in the standard-cell library, it is meaningful only in designs in which digital logic dominates and leakage power is a significant component of the total power.

Another aspect of power management that engineers sometimes overlook is power integrity. Power integrity affects both the core and the I/O power in a chip. You must take care to distribute the power in the core, especially in the case of a multiple-power-supply design and when the external power delivery is by means of a wire-bond package. In a typical flip-chip design, the availability of a large number of bumps, especially in the core region of the chip, enables distribution of power to the core with minimal IR (current/resistance) drop and minimal signal-integrity effects. For a wire-bond package, however, you must perform careful analysis to ensure that you have allocated enough I/O buffers for power and ground to accommodate the core power requirements.

IR drop and EM (electromigration) are other key areas of concern in the core region. You must ensure that the worst-case supply voltage in the core region does not fall below 10% of the nominal value, meaning that the total variation in power supply across the package and the die should not exceed 10%. The external supply itself typically has 5% tolerance, which means that you typically need an IR drop of 5% or better on the die. Otherwise, you must have a smaller tolerance on the external supply, which significantly increases the cost of its voltage regulator. This requirement often dictates the number of power and ground I/O buffers on the die and the choice of the thickness and width of the top metal layers on which you will design the power mesh.

In addition to IR drop, you must satisfy the EM criteria. The EM current-density limit is the current density above which metal migration occurs, resulting in irreversible damage to the metal layer and eventually causing an open connection. The EM current densities are significantly tighter at higher temperatures. For example, a 10° increase in operating temperature from 110 to 120°C requires a doubling of the metal-trace width because the EM-current-density limit at 120°C is only one-half of the limit at 110°C. So you must take into account the EM criteria at the maximum operating temperature of the die when you determine the number of I/O buffers for power and ground.

Finally, you will need to insert decoupling capacitors in the core—and sometimes in the package—to smooth out large peaks in the core current. Also, when a chip includes multiple power domains in which large blocks of logic switch off and on, a key design consideration is to ensure that there is enough decoupling capacitance or phase management to ensure the integrity of the turn-on operation during any sudden surge in operating currents. There is generally plenty of room available for such devices on the core. Most standard-cell libraries provide decoupling-capacitor cells that you can place in the unused portion of the standard cell regions in a chip. In addition, you can build custom cells for use in other areas of the chip. Note that you must design decoupling-capacitor cells with low leakage, however, because they can otherwise contribute to significant additional leakage. This leakage can be a challenge because lower leakage also means lower capacitance. EDN

AUTHOR'S BIOGRAPHY

Prasad Subramaniam, PhD, is vice president of design technology at eSilicon Corp, where he is responsible for developing the technology platforms for IC design. He has a wide range of experience in ASIC, custom, and mixed-signal design. Subramaniam is a senior member of the IEEE and has published more than 40 papers in technical conferences and journals. He received a doctorate in electrical engineering from the State University of New York—Stony Brook.

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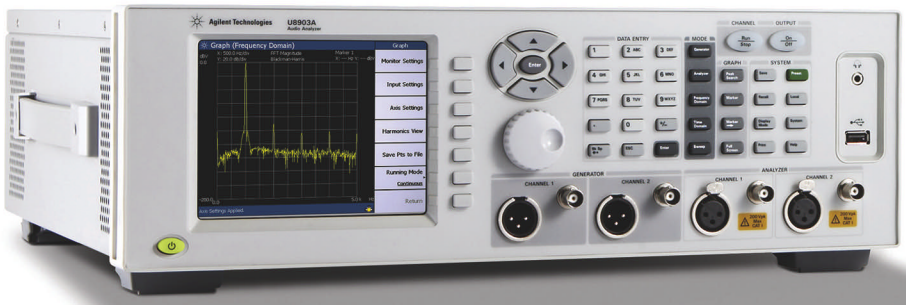

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READERS SOLVE DESIGN PROBLEMS

Photoresistor provides negative feedback to an op amp, producing a linear response

Julius Foit and Jan Novák,
Czech Technical University, Prague, Czech Republic

AGC (automatic-gain-control) amplifiers use the nonlinear characteristics of control devices. The magnitude of the real component in some of their differential parameters changes depending on variations in their dc operating points. A typical example is the VA characteristic of a silicon PN junction, which results in the differential conductance directly proportional to the passing dc current (**Reference 1**). In this form of control, the main problem is the control element's nonlinear transfer characteristic, which causes a relatively large degree of nonlinear signal distortion once the processed voltage amplitude exceeds millivolts (**Reference 2**).

A photoresistor, which has a VA characteristic that's linear in a large range of voltages, is up to the task. Common photoresistors remain perfectly linear for signal amplitudes of 100V or more. Therefore, the amplification-control device can be an optocoupler whose controlled element is a photoresistor.

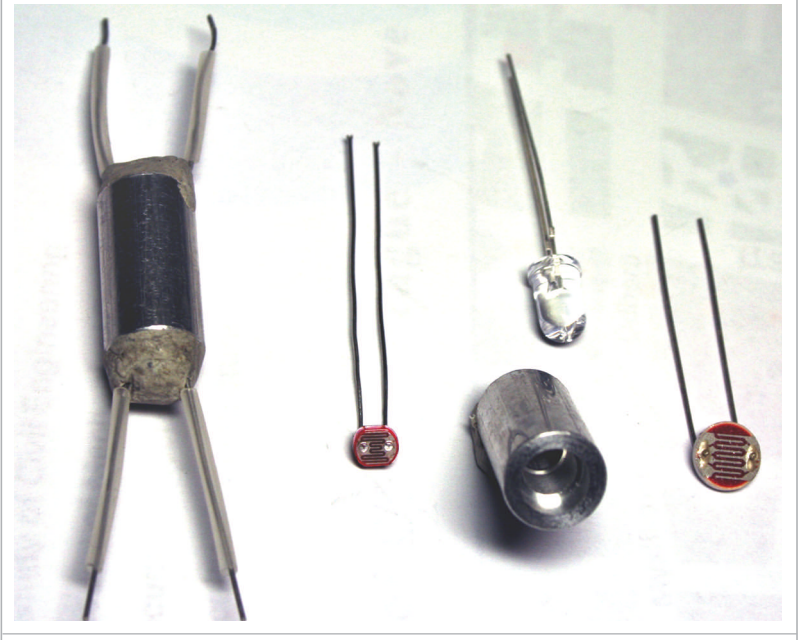

Figure 1 A metal tube with an HB LED and a photoresistor forms the optocoupler (left).

DIs Inside

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The circuit in this Design Idea uses a radiation source whose spectral characteristic fits the spectral characteristic of the photoresistor, and its radiated power should, if possible, be a linear function of the drive signal. Such optocouplers are commercially available, but few have properties good enough for this purpose. Common photoresistors have spectral characteristics close to the spectral characteristics of the human eye, whose peak sensitivity has approximately a 500-nm wavelength. So a white or green LED (light-emitting diode) is a good alternative. To obtain the highest possible sensitivity, this circuit uses a white HB (high-brightness) LED.

Figure 1 shows the individual components of the optocoupler and the assembled device. The optocoupler comprises a cylindrical holder that accepts a standard 5-mm HB LED from one end and a photoresistor at the other end. An opaque nonconductive seal prevents external light from entering the device. The polished metallic inner wall of the holder results in minimum light loss between the LED and the photoresistor. Available off-the-shelf photoresistors include the LDR 05, the LDR 07, and a standard white, 5-mm HB LED type L-53MWC*E, with output-light flux of 2500 mcd at a 20-mA drive current (**Reference 3**).

Figure 2 shows the transfer function of the optocoupler using the LDR 07-type photoresistor. The output resistance of the device can vary from 100Ω to 10 MΩ with LED-drive currents from 34 mA to 0.1 μA, respectively. The photoresistor's linear VA characteristic, even for large-amplitude signals, lets you use it as the control element even in situations that require a relatively large signal voltage, such as when the photoresistor is part of the feedback loop of an operational amplifier. **Figure 2** also shows that you can obtain a variation of linear output resistance over at least five decades with a maximum LED-drive current within the limits of permitted output current of common monolithic operational amplifiers.

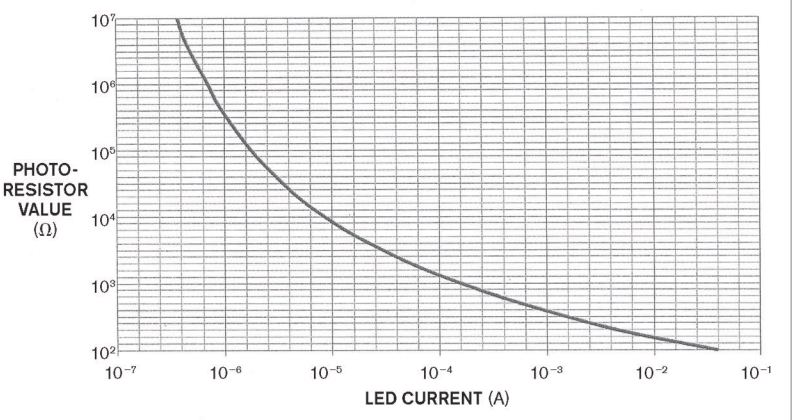

Figure 2 The optocoupler's logarithmic response in a feedback loop produces a linear amplifier response.

Such an amplifier can control the overall amplification of the system in the same range without additional current amplification. Due to the photoresistor's linearity, the resulting degree of processed signal nonlinear distortion is almost solely due to the nonlinearity of the operational amplifier. Within the normal operating range, the overall linearity of the system improves with increasing input-signal amplitude because the amount of negative feedback increases with increasing signal amplitude.

Figure 3 shows the amplifier system. The basic signal-processing device is inverting op amp A_1. Its inverting connection lets you set the absolute value of the overall amplification from input to output to a value smaller than unity, permitting correct processing of an input-signal amplitude even larger than the regulated output value. Optocoupler IC_1 is the core component of the system, whose output, the photoresistor, serves as a variable part of A_1's negative-feedback network. At no-signal conditions, the LED does not illuminate the photoresistor. Thus, its resistance rises to a high value, which can cause dc runaway and the loss of the quiescent operating point of A_1. Such a condition is not harmful in principle because the signal path is ac-coupled, preventing the dc error value from getting any further. When a nonzero signal suddenly appears at the input, however, A_1's open-loop amplification would amplify it, causing a rapid rise in LED current. This action would drop the optocoupler's output resistance almost stepwise to a value sufficient to restore the dc operating point of A_1. The ac coupling transfers this transient to the output, and it may cause problems in signal-processing circuits following the adaptive amplifier. To prevent this effect, you should limit the maximum value of the feedback resistance to a reasonable value, such as 47 MΩ,

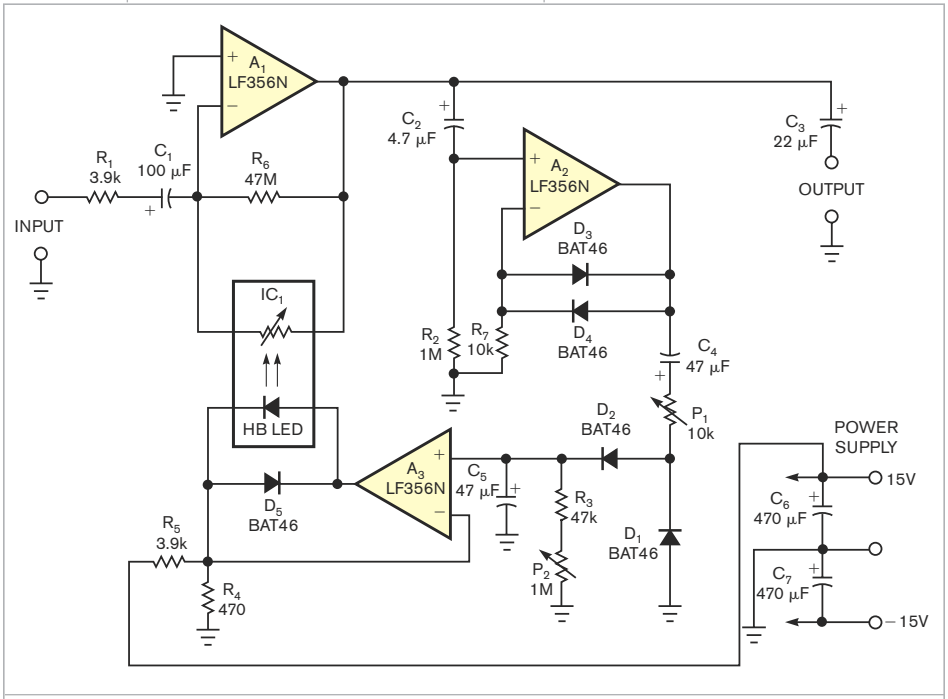

Figure 3 The adaptive-amplifier system has the optocoupler in a feedback loop.

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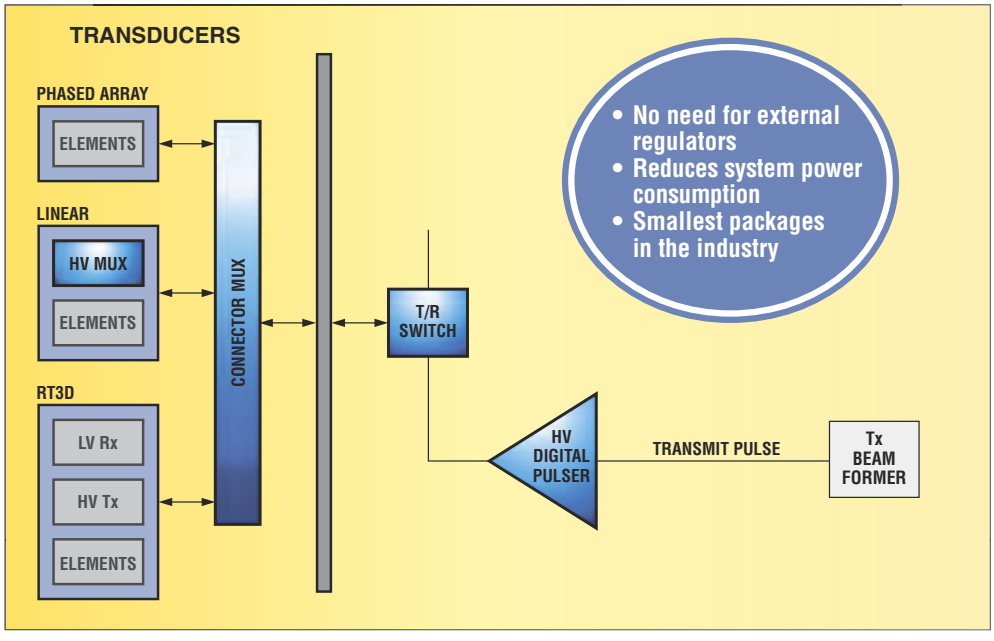

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the value of R_6. Because the op amps have JFET inputs, the value of R_6 can be rather high. The value of 47 MΩ is a reasonable compromise, limiting the maximum absolute value of voltage amplification in A_1 to approximately 82 dB. The limiting factors for selecting a value for R_6 are the noise and the open-loop amplification of A_1.

Buffer A_2 separates the nonlinear load through the rectifying diodes from the output signal, thus preventing the nonlinear load from the rectifying diodes from distorting the output signal. Diodes D_3 and D_4 compensate the threshold voltage, including its temperature coefficient, of rectifying diodes D_1 and D_2. If you do not need to set the regulated output-voltage amplitude to a value smaller than the threshold value that the bias current in R_4 sets, you can replace D_3 and D_4 with a short circuit and omit R_7. You can set a larger-than-unity voltage amplification in A_2 to obtain a regulated output amplitude lower than the threshold that the bias in R_4 sets. Just insert an additional resistance in series with the D_3/D_4 pair.

The rectifier uses Schottky diodes, which have a lower threshold voltage than conventional PN diodes. They also have a short recovery time, keeping the same rectification efficiency at high signal frequencies. The rectifier operates as a full-wave voltage doubler, providing peak-to-peak rectification even for signals with nonsymmetrical waveforms. The rectifier output feeds to A_3, a voltage-to-current converter, which drives the LED in the optocoupler. A rectification threshold-shifting bias-current source connects to current-sensing resistor R_4. In this case R_5 simulates a current source, setting the regulated output-voltage amplitude. If the 15V supply voltage isn't perfectly stable, obtain bias current from a separate stable source. An opposite-polarity diode connects across the optocoupler's input to protect the LED from reverse polarization at no-signal conditions.

This LED current-control circuit has an important advantage: It permits an almost-independent adjustment of the attack and release time. You can adjust the attack time through variable resistor P_1, using a higher value if necessary. You can also adjust the release time using P_2. The photoresistors used have a rather good response speed, and the introduced delay at a stepwise illumination variation is acceptable for most practical requirements.

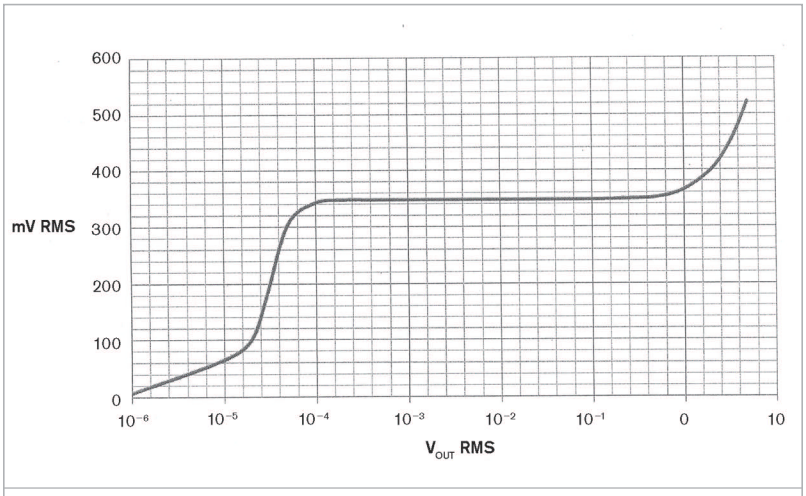

Figure 4 The amplifier system has a constant output from 0.1 mV to 1V-rms input.

Figure 4 shows the overall response of the adaptive amplifier system. The output signal remains constant at 350 mV rms ±1 dB for input-signal voltages of less than 70 µV rms to more than 1.2V rms—that is, over a more-than-85-dB range. The no-signal output noise is less than 6 mV rms, yielding an SNR (signal-to-noise ratio), or processed-signal dynamic range, better than 20 dB at the onset of regulation in the worst-case condition and improving proportionally with increasing input-signal level.

The key parameter this design follows is its linearity. Because of the photoresistor's linearity and the separation of the nonlinear rectifier load from the output, the gain control introduces negligible nonlinearity. Thus, A_1 alone, in principle, determines the overall linearity of the system.

Harmonic analysis of the output signal at 1 kHz yields higher harmonics with amplitudes lower than A_1's noise level for all input voltages to 200 µV rms and below −75 dB for input voltages to 1.5V rms. The nonlinear distortion becomes noticeable only at large input amplitudes exceeding the regulation range of the system, raising the second harmonic to −45 dB and the third harmonic to −40 dB at 2.5V-rms input.

Within the AGC's range limits, the overall transfer linearity improves with increasing input-signal amplitude due to the increasing degree of negative feedback to A_1 at increasing input-signal amplitudes. With a value of 10 kΩ for P_1 and 1 MΩ for P_2 and a stepwise input-signal variation between 100 µV and 50 mV rms, the attack and release times are approximately 0.2 and 2 seconds, respectively. The recovery time from a 1-kHz—more than 10V-rms input overdrive—to full no-signal sensitivity is less than 2 minutes. You can adjust all of these time intervals in a wide range by varying the values of C_4, C_5, P_1, and P_2, with P_1 setting the attack time and P_2 setting the release time. EDN

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3 *Opto-isolator Catalogue*, Tesla Blatná, www.tesla-blatna.cz.

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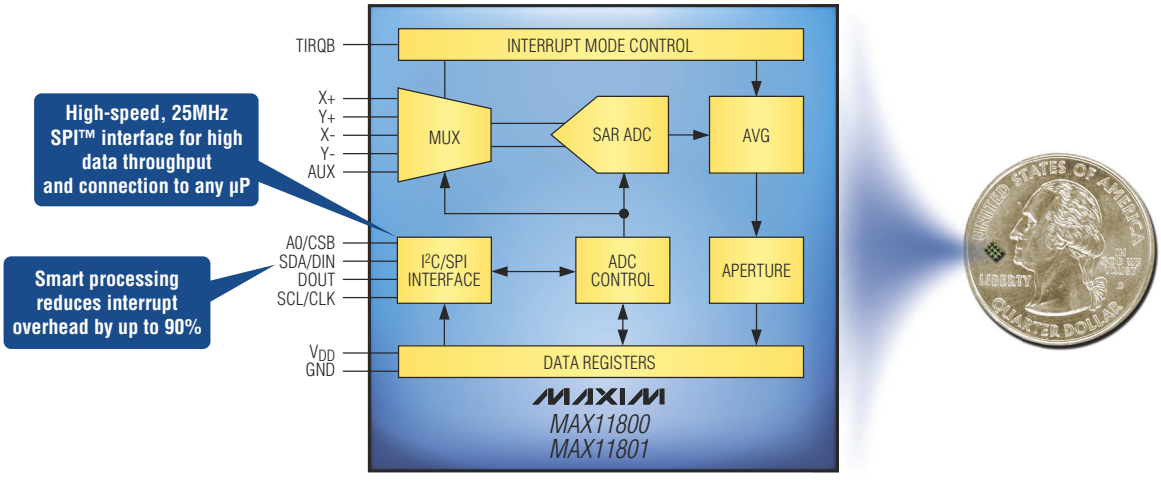

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Three-phase digital-signal generator sweeps frequency

Yi-Chu Liao and Shao-Wei Leu,
National Taiwan Ocean University,
Keelung, Taiwan

Many power ICs use frequency jitter, which spreads a control signal's spectrum, to control EMI (electromagnetic interference). If you need to add frequency jitter to power ICs that control three-phase signals, you can use an FPGA and the code in this Design Idea, which is available at www.edn.com/100527dia. The digital three-phase signal sweeps over a 20-kHz range of 100 to 120 kHz and back in 40 steps in 500 msec (**Figure 1**). The basic clock frequency can range from 600 to 720 kHz. You can develop the three-phase generator using Verilog (www.verilog.com) HDL code and Altera (www.altera.com) FPGAs.

The three-phase generator starts with a 50-MHz clock and ends with three output phases (**Figure 2**). The circuit's two main parts are the sequential frequency-scanning part and the three-phase model. The frequency-scanning part comprises the frequency model and Model 2 blocks. The sequential frequency-scanning part generates a frequency of 600 to 720 kHz. The three-phase model receives the variable clock-period frequency from the output of Model 2. One phase period comprises six clock periods from the three-phase input frequency. The relations of phases 1, 2, and 3 are 101, 100, 110, 010, 011, and 001, respectively, over six clock pulses. Together, they construct a three-phase waveform with a 120° phase difference.

Using the source code, you can implement the circuit using the Altera FPGA DE2 development tool, which has a basic frequency of 50 MHz, to control these circuits. The three-phase frequency sweeps in 40 1-kHz steps from 100 to 120 kHz and back in 0.5 seconds (**Figure 3**). The sequential frequency-scanning part generates an 80-Hz, 20-steps-up/20-steps-down sweep

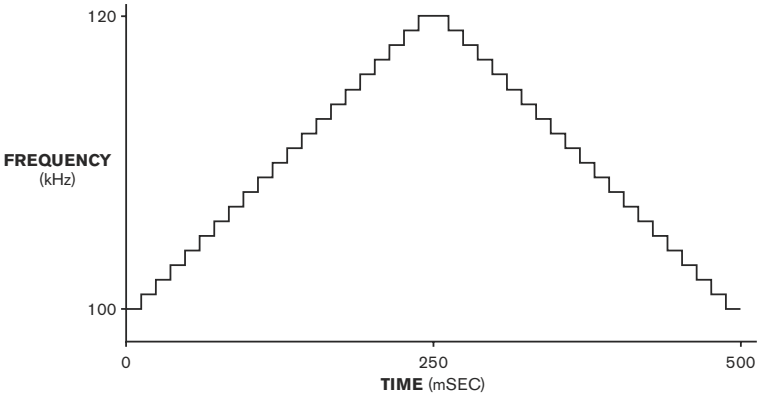

Figure 1 This digital three-phase signal sweeps over a 20-kHz range of 100 to 120 kHz and back in 40 steps in 500 msec.

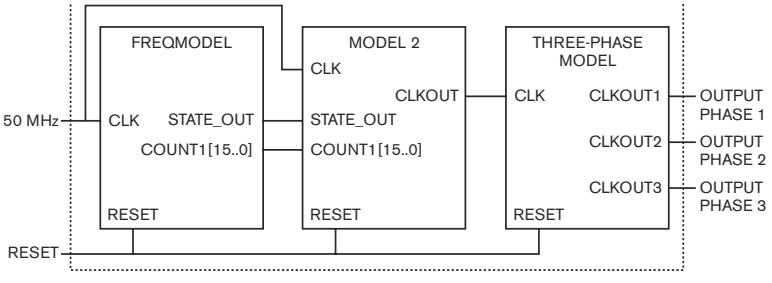

Figure 2 The three-phase generator starts with a 50-MHz clock and ends with three output phases.

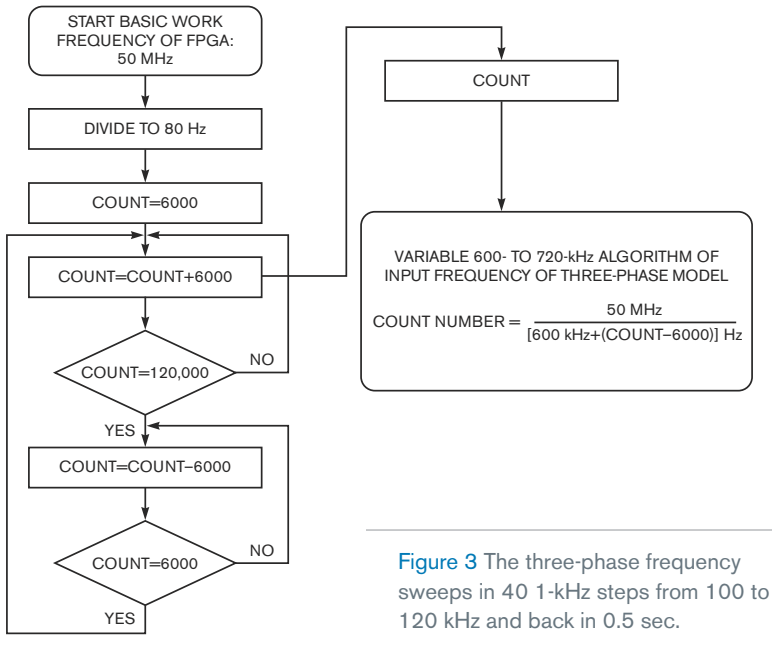

Figure 3 The three-phase frequency sweeps in 40 1-kHz steps from 100 to 120 kHz and back in 0.5 sec.

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by the internal divider from the 50-MHz basic frequency. To obtain the 100- to 120-kHz frequency as the output frequency of the three-phase signal, you first generate clocks of 600 to 720 kHz as the input clock of the three-phase generator because one of the output-phase clock periods should be in six equal periods of 60°. The following **equation** shows how to get the frequency shift from the basic signal frequency:

$$100\,\text{kHz} \leftrightarrow 120\,\text{kHz} = \frac{600\,\text{kHz} \leftrightarrow 720\,\text{kHz}}{6}.$$

The first phase starts on the positive edge of the first period, and the second phase starts after two periods of the input clock at the positive edge. The second phase now lags by two input clock periods, or 120°. The third phase then starts after two more input-clock periods. The counter starts with a value of 6000 because the period of the three-phase model requires six clock times, and the sweeping frequency is 1 kHz. The **equation** in **Figure 3** shows how the count number derives from the 50-MHz clock signal.

The counter increases in value to 6000 in 0.0125 seconds, or 80 Hz, until it reaches 120,000. The count then decreases back to 6000. The variable "count" is the input to the Model 2 block, which generates clocks of 600 to 720 kHz—the input-clock period of the three-phase block. Finally, the three-phase frequency changes in sequence, counting up from 100 to 120 kHz and back down to 100 kHz in 1-kHz steps over 0.5 seconds. **Figure 4** shows the relationships among the three phases.

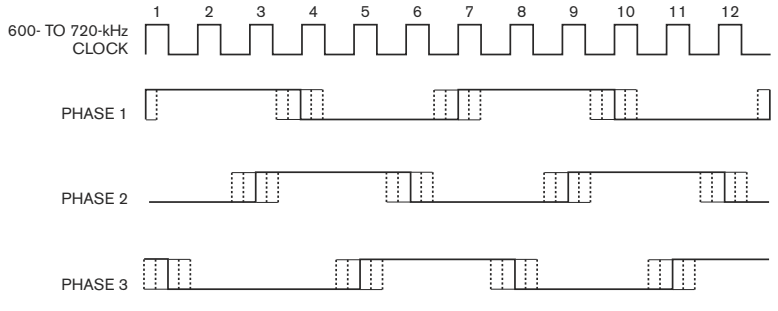


Figure 4 The three-phase frequency changes in sequence, counting up from 100 to 120 kHz and back down to 100 kHz in 1-kHz steps over 0.5 seconds.

Using this algorithm, you can develop and implement a lightweight, low-cost, three-phase signal with a 120° relative phase difference and simultaneous sweeping on one FPGA chip. You can use three lowpass filters to create sine-wave signals from the outputs. EDN

Water-leak detector uses 9V batteries

Yongping Xia, Navcom Technology, Torrance, CA

A previously published Design Idea describes a practical gadget that has the potential to save a lot with little investment (**Reference 1**). However, the circuit uses 120V line voltage and, as such, it is not that convenient for many applications. This Design Idea describes a portable water-leak detector that uses a common 9V battery for power (**Figure 1**). The circuit consumes less than 10 µA during detection mode, and a 9V alkaline battery has greater-than-500-mAhr capacitance. So one battery can last more than five years, which is equivalent to the battery's shelf life. When the battery voltage drops below 6.5V, the detector beeps to indicate that it is time to change the battery.

The design uses Maxim Integrated Circuits' (www.maxim-ic.com) MAX934, an ultra-low-power quad comparator with a built-in 1.2V reference. The chip uses about 6 µA. IC_{1A}, R_1, and R_2 provide water-leakage detection. R_1 is the water probe, which can be two bare copper wires wrapped in a sponge. R_1 has high impedance when the sponge is dry, so IC_{1A}'s output stays high. Once the circuit detects the water leak, R_1's value decreases to less than a few hundred kilohms, which forces IC_{1A}'s output low. Through D_1, it makes the output of IC_{1B} high.

THIS PORTABLE WATER-LEAK DETECTOR USES A COMMON 9V BATTERY.

IC_{1B}, R_3, and R_4 form a low-voltage detector. When the water probe is dry and the battery voltage becomes lower than 6.6V, the voltage on IC_{1B}'s negative input is less than 1.2V. Because the reference voltage is 1.2V, IC_{1B}'s output changes from low to high. So when the probe is dry and the battery voltage is higher than 6.6V, IC_{1B}'s output is low, which forces IC_{1C}'s output high, and IC_{1D}'s output stays low.

Either a wet probe or a low-voltage battery can force IC_{1B}'s output high, freeing a narrow-duty-cycle oscillator comprising IC_{1C}, C_2, R_5, R_8, and D_3. The oscillation period is approximately 7 seconds, and IC_{1C}'s output is low for about 0.3 seconds. That low output allows a 2.4-kHz oscillator comprising IC_{1D}, C_3, and R_9 to operate. When the circuit detects a water leak or the battery's power is low, the buzzer sounds for a fraction of a second every 7 seconds. In this way, the warning sound can last for a long time before the battery gets too low.

Resistors R_6 and R_7 increase IC_{1C}'s hysteresis, which lets you use a smaller value for C_2. R_{10} and R_{11} increase IC_{1D}'s hysteresis to improve the sound frequency's stability. All capacitors are ceramic, ensuring low leakage current. **EDN**

REFERENCE

Tregre, Jeff, "Doorbell transformer acts as simple water-leak detector," *EDN*, Dec 15, 2009, pg 48, www.edn.com/article/CA6711862.

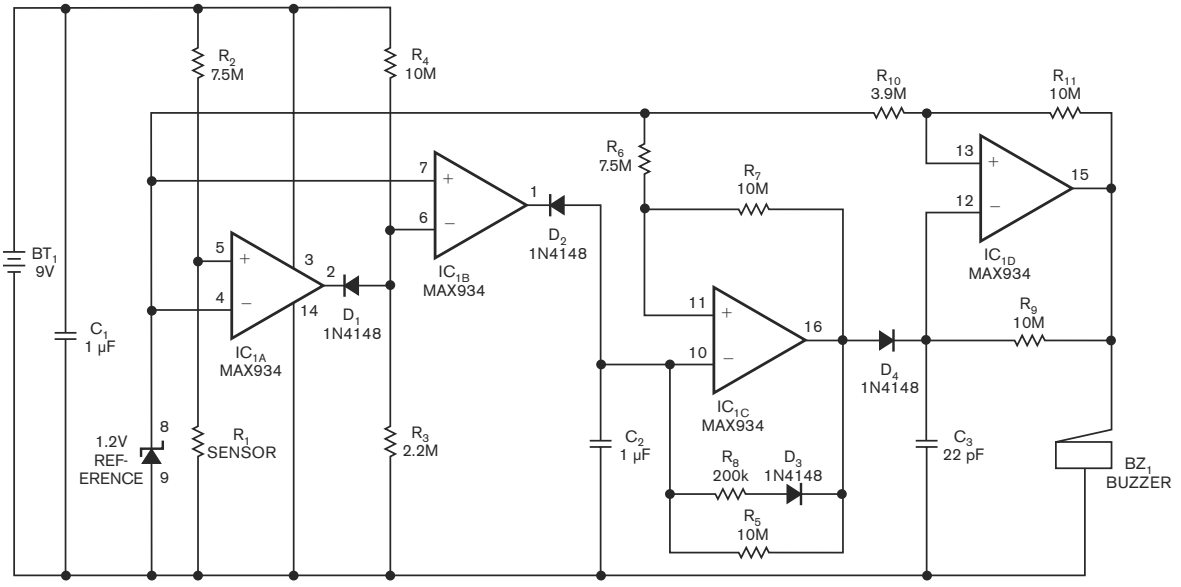
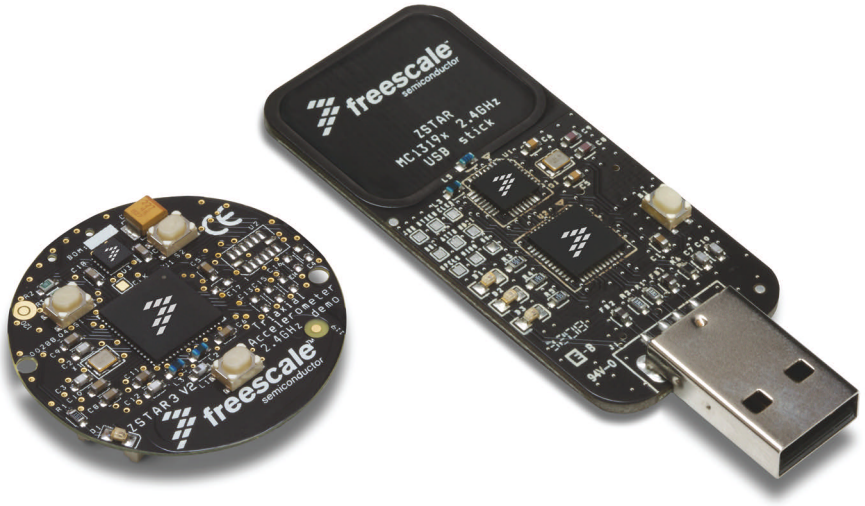


Figure 1 IC_{1A} and IC_{1B} determine the conditions for sounding the buzzer, and IC_{1C} oscillates to provide the trigger for IC_{1D}.

productroundup

SENSORS/TRANSDUCERS



Reference design features shake and tap detection for consumer applications

The wireless ZSTAR (ZigBee triple-axis-reference) demonstration collection features the MMA7660FC triple-axis accelerometer and targets use in mobile phones, small appliances, and gaming. The accelerometer also has built-in intelligence for orientation, shake, and tap detection. It includes smart power-management features, such as automatic wake-up and sleep modes to extend battery life. The RD3965MMA7660FC ZSTAR reference design provides designers with two small, portable demo boards; a sensor-transceiver board; and a USB-receiver board for evaluating and demonstrating a range of accelerometer-based applications with low-power wireless connectivity. A USB stick connects through the computer's USB port for communications using the vendor's full-speed, 8-bit USB 2.0 MC68HC908JW32 microcontroller. The RD3965MMA7660FC ZSTAR reference board is available for $99.

Freescale Semiconductor, www.freescale.com

Programmable, triple-axis MEMS vibration sensor monitors equipment condition

The triple-axis embedded ADIS16223 iSensor accelerometer/digital vibration sensor enables simple, effective, and affordable monitoring of manufacturing equipment. The sensor combines MEMS technology with signal processing, data capture, and an SPI. The SPI and data buffer provide access to wide-bandwidth sensor data. The sensor offers 22-kHz resonance and a 72.9k-sample/sec sample rate. The programmable digital filter offers lowpass- and bandpass-configuration options. The ADIS16223 has a ±70g dynamic range across three axes and sells for $145 (1000).

Analog Devices Inc, www.analog.com

Hall-effect latches have high voltage-transient protection

The A1225, A1227, and A1229 Hall-effect latches operate at temperatures as high as 150°C and target use in applications requiring high voltage-transient protection close to the sensors in the system. They provide as much as 8-kV HBM (human-body-model) ESD protection without external protection components. Internal protection circuits enable the devices to survive 40V load-dump compliance. The devices target use in motor-commutation applications in automotive sunroofs and power windows. Each device comprises one chip that includes a voltage regulator, a Hall-voltage generator, a temperature-compensation circuit, a signal amplifier, a Schmitt trigger, and a buffered open-drain output to sink as much as 25 mA. The onboard regulator permits operation with supply voltages of 3.8 to 24V. The A122xLLTTR-T operates at −40 to +150°C and comes in a miniature SOT89/TO-2433A transistor package for surface-mount applications. It sells for 51 cents (1000). The A122xLUA-T operates at −40 to +150°C, comes in a three-lead ultramini SIP, and sells for 60 cents (1000).

Allegro MicroSystems Inc, www.allegromicro.com

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POWER SOURCES

One-eighth-brick power module optimizes 5V bus voltage to match load requirements

The BMR454 0002/004 one-eighth-brick power module has typical efficiencies of 94 and 93.5% at 50 and 100% loads, respectively. The devices deliver 38A at 5V or a maximum output power of 190W across their operational range of 36 to 75V. To minimize power losses at the application level, designers can dynamically adjust the voltage from 3 to 6.7V through the PMBus, accommodating intermediate-bus voltages to the conditions that POL, FPGA, and ASIC applications require—without energy losses during conversion. Externally set the output voltage using an additional resistor. A 3.3V-output version, BMR454 0002/0003, delivers 3.3V at 40A and 132W. The BMR454 offers a power-density figure of more than 14W/cm^2. The BMR454 0002/004 sells for $37 (OEM quantities).

Ericsson Power Modules, www.ericsson.com/powermodules

Proximity-detection devices operate behind darkened glass

The TSL2771 family of digital ambient-light-sensing and proximity-detection sensors eliminates the need to use clear glass or plastic in front of a sensor or drill holes in a display, bezel, or frame. The TSL2771 device family instead operates behind darkened glass or other translucent materials, providing both ambient-light sensing and proximity detection. The devices incorporate an IR LED current-limited drive, analog-to-digital conversion, interrupt capability, and multiple I^{2}C-interface-voltage options. The TSL27711 and TSL27713 sell for $1.07 (1000). The TSL2580 with an SMBus interface and the TSL2581 with an I^{2}C interface are available in FN packages and sell for 75 cents each (1000).

Texas Advanced Optoelectronic Solutions, www.taosinc.com

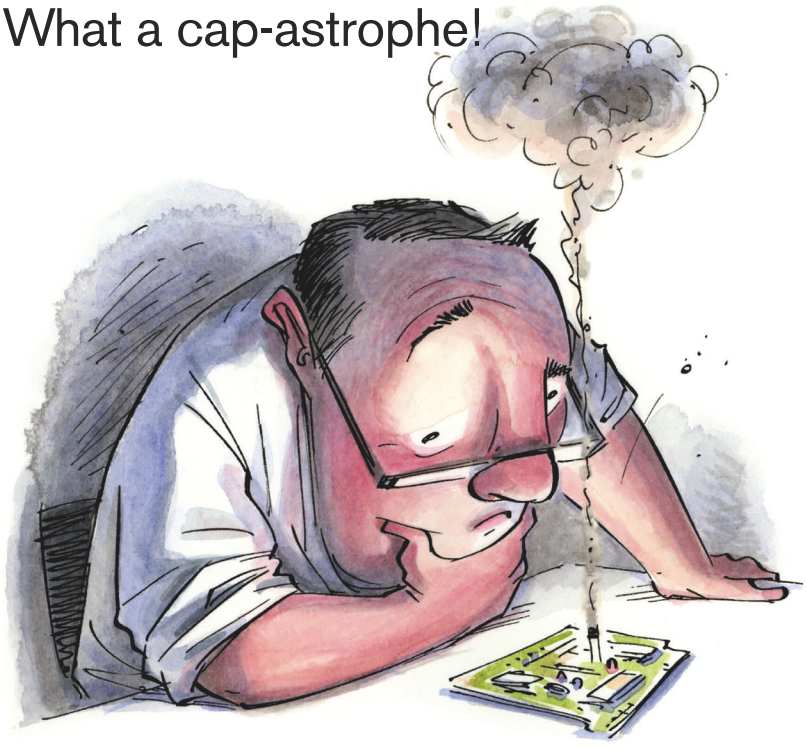
Quad-output ac/dc power supplies feature four adjustable outputs

The LPQ200-M series open-frame, ac/dc power supplies feature four adjustable outputs. The devices measure 3×5 in. and are 1.32 in. high—fitting into a profile smaller than 1U. Power density is more than 10W/in.^{3}, and the devices can achieve efficiency as high as 84% at full load. The LPQ201-M offers outputs of 3.3, 5, 12, and −12V, and the LPQ202-M offers dc outputs of 5, 12, 24, and −12V. Input voltages range from 90 to 264V ac. The devices sell for $149 each (production quantities).

Emerson Network Power www.emersonnetworkpower.com

JIM KEITH • ENGINEERING CONSULTANT

What a cap-astrophe!



I was working at a manufacturer that was experiencing unexplained tantalum-capacitor failure. It wasn't that the capacitors were just failing, but the failure was catastrophic and was rendering PCBs (printed-circuit boards) unfixable. There seemed to be no explanation. We found no misapplication issues for this small, dedicated microcomputer PCB. Worse yet, the supplier blamed us.

The capacitor application was a dc input-power-bypass function. Some analysis indicated that the units had significant ripple current, but it was well within its current rating. The temperature increase was only 13°C over the rated 40°C ambient—far below the 85°C capacitor specification. The operating voltage was 27V—far below the rated voltage of 50V, so there was no issue there.

The first break came when we observed two failures that were not catastrophic; part of the chip capacitors remained intact. I sent one capacitor that had blown off the PCB and one complete PCB to the capacitor vendor for analysis, which in turn sent them offshore to the manufacturing division. The division came back with a plausible diagnosis: A serpentine burn pattern on the pellet clearly indicated excessive voltage.

I did some Internet research on tantalum-capacitor failures and found that the tantalum capacitors' pellets contain minor defects that must be cleared during manufacturing. In this process, the voltage is increased gradually through a resistor to the rated voltage plus a guardband. The series resistor prevents uncontrolled thermal runaway from destroying the pellet. I also learned that soldering PCBs at high temperatures during manufacturing causes stresses that may cause microfractures inside the pellet. These microfractures may in turn lead to failure in low-impedance applications. The microfractures also reduce the device's voltage rating so that failure analysis will indicate classic overvoltage failure.

Lead frames reduce this stress on the pellet to improve reliability. Pellets without lead frames must be soldered directly to the PCB, thus causing mechanical stress; this stress increases substantially with pellet size. Modern construction techniques for large tantalum capacitors use multiple smaller pellets that connect to a common lead frame. We had all these conditions simultaneously—large pellets, no lead frames, a low-impedance voltage source, and overvoltage failure.

A second break came unexpectedly when a service tech noted that the first-generation artwork was reliable. Further checking revealed the first-generation PCB paralleled four 6.8-µF tantalum capacitors, whereas the later ones paralleled two 6.8-µF capacitors and one 15-µF capacitor to save board space. The 15-µF capacitor was the one that was failing.

Now we had the probable cause, but no solution. The supplier remained unresponsive, and we were stuck with the product because it was application-specific. Having no control over the product, how could we possibly solve the problem or take care of all units in the field?

I had the idea to build a capacitor-postprocessing fixture. Its function was to slowly ramp up the voltage applied to the PCB with enough current capacity to power everything on the PCB but with sufficient internal resistance to limit transient capacitor-clearing fault current. Surprisingly, the postprocessing fixture worked! No failures occurred during postprocessing of the units in stock or those in the field. This finding demonstrated that the series element successfully limited clearing-fault current, assuming that 10 to 20% of the units perhaps would fail.

The proof was in the pudding: We went from about one or two failures per month to more than 18 months without a single failure. Works for me! EDN

Jim Keith is an engineering consultant in York, PA.

DANIEL VASCONCELLOS

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LTC4070	Nanoamp operating current shunt Li-Ion battery charger	

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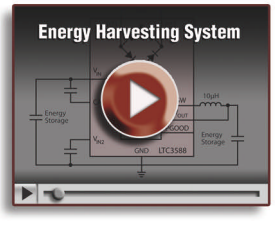

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